OBJEX

ELPM-N54LW

Extreme Low Power Module based on nRF54L15 and SX1262

v1.0 LW-B

DATASHEET

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Contents

1 | Overview

The ELPM-N54LW is an extreme-low power module based on the nRF54L15 and the SX1262, designed especially for battery-powered and energy-harvesting IoT applications. Its low-power 2.4 GHz radio, Sub-GHz radio, configurable power unit and Deep Stop mode support systems that must minimize both active and standby energy. The module also integrates an ATECC608C secure element for hardware-protected keys and cryptographic operations.

1.1 | Features

Microcontroller

- Based on nRF54L15
- 128 MHz Arm Cortex-M33 with DSP and FPU
- 1524 KB NVM (RRAM) and 256 KB RAM
- 128 MHz RISC-V coprocessor for SoftPeripherals
- Bluetooth LE, Bluetooth Mesh and Bluetooth Channel Sounding
- IEEE 802.15.4, Thread, Zigbee and Matter
- Proprietary 2.4 GHz modes up to 4 Mbps
- TrustZone, tamper detection and cryptographic engine
- NFC interface on NFC1/NFC2 pins for an external antenna
- Red status LED: nRF54L15 P2.03
- Low-power-domain I²C bus on P0.04/P0.02, with integrated 10 kΩ pull-up resistors to VMCU
- U.FL connector (GHz): multiprotocol 2.4 GHz radio, 50 Ω

Sub-GHz radio

- Based on SX1262
- Frequency bands: 862 MHz to 928 MHz
- Max output power: +22 dBm
- Transmission distance: up to 5 km (antenna and environment dependent)
- Air data rate: LoRa up to 62.5 kbps, (G)FSK up to 300 kbps
- TX current: 118 mA @ +22 dBm (typ)
- RX current: 4.6 mA (typ)
- U.FL connector (SUB_GHz), 50 Ω matched output
- Direct external supply through the VSUB pad
- Full compatibility with LoRa, LoRaWAN and generic Sub-GHz protocols

Extreme-low power unit

- Direct VMCU rail supplies the nRF54L15 and ATECC608C
- WAKE and MASTER inputs: rising/falling edge detectors triggering the power latch
- 1-30 nA battery draw in Deep Stop (power latch only)
- WAKE/MASTER inputs: 3.3 V max, high value resistance to GND (not floating)
- RTC RV-3028-C7: 45-100 nA when used as Deep Stop wake source
- Dedicated RTC power supply pad
- Battery-level input on P1.06 through a 2 × 100 kΩ resistive divider[a]

[a] A future hardware revision is planned to use the nRF54L15 internal battery-level measurement, removing the divider and making the GPIO available.

Security

- ATECC608C secure element
- Hardware secure key storage
- ECDSA sign/verify, ECDH (ECC P-256)
- SHA-256, AES-128
- User-configurable secure memory slots

1.2 | Deep Stop Mode (Extreme low power)

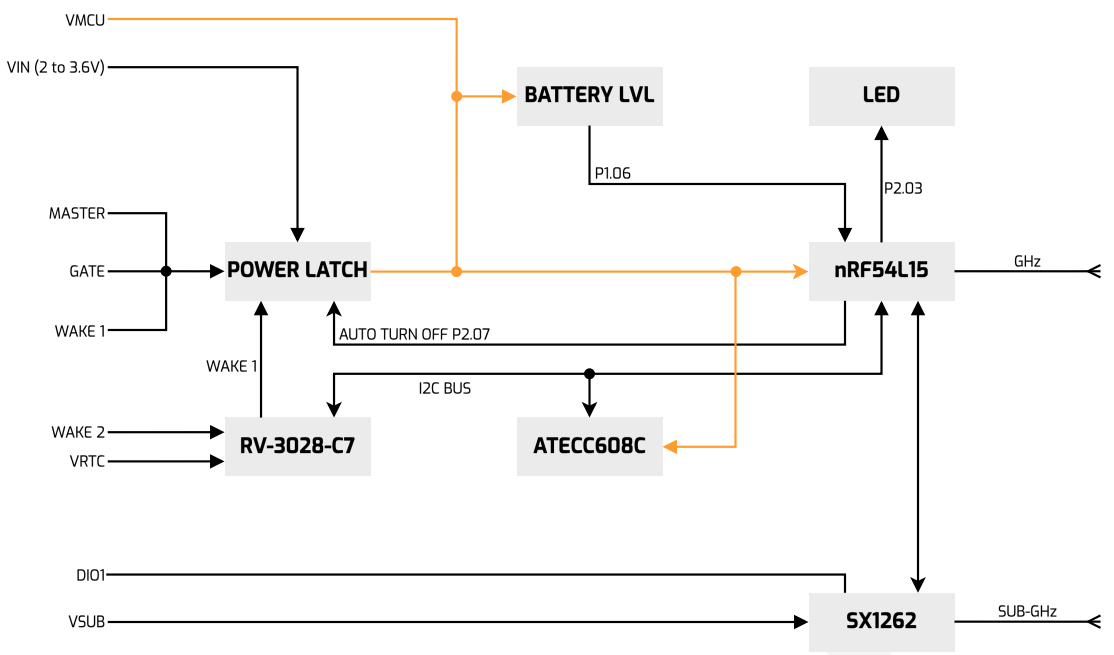
Deep Stop is an extreme-low power alternative to the nRF54L15 System OFF and sleep modes. A power latch, triggered by the RTC or by the WAKE/MASTER inputs, removes the main supply from the nRF54L15 and every load on the switched VMCU path. The GATE node can control an external MOSFET to switch additional loads with the latch and may also be pulled low externally to force power on. Details are provided in Section 6.

1.3 | Applications

The ELPM-N54LW fits a wide range of low-power applications, including the ones listed below. For some of them, ready-to-use KiCad reference designs (schematic and pre-configured project) are available in the OBJEX Labs GitHub repository: the linked applications can be clicked to download the corresponding project.

- Battery-powered nodes
- Smart meters
- Asset tracking
- Personal-item tracking tags for compatible crowd-sourced finding networks
- Smart cities
- Street lights
- Supply chain
- Building automation
- Energy harvesting
- Smart agriculture
- Environmental sensors
- Predictive maintenance
- Cold chain monitoring
- Smart locks and access control
- Structural health monitoring
- Waste management
- Wireless alarm systems

2 | Block diagram



VMCU: Direct supply input for the nRF54L15 and ATECC608C rail, bypassing the power latch. The module does not regulate this rail; the external source must remain within the specified VMCU range.

MASTER: Power latch input: if the status changes (0 to 1 or 1 to 0), the power latch is triggered.

GATE: Bidirectional power-latch control node. It follows the internal latch state and can control the gate of an external MOSFET so that additional loads switch with the module. It may also be pulled low externally to force the power latch on.

WAKE: Power latch input: if low, the power latch is triggered with a short startup delay.

DRAIN: Unregulated switched copy of VIN and the main switched module supply. Its voltage is nominally equal to VIN apart from the internal path drop, and the pin becomes high-impedance when the latch is off.

AUTO TURN OFF: In VIN power-latch mode, this firmware-controlled signal holds the latch on when high and requests shutdown when low. While held high, further MASTER, WAKE and GATE events are ignored. It does not control the supply in direct VMCU mode.

VRTC: External supply for the RV-3028-C7. The module has no internal RTC backup battery; removing VRTC stops timekeeping and the stored date and time are lost.

WAKE1: Direct external input to the power-latch wake path.

WAKE2: External event input of the RV-3028-C7. When VRTC is supplied, an event on this pin or an internally programmed RTC timer/alarm asserts RTC INT, which reaches the same power-latch wake path.

VSUB: Direct external supply input for the SX1262. The module does not regulate this rail.

STATUS LED: Controlled by nRF54L15 P2.03.

3 | Pin Definition

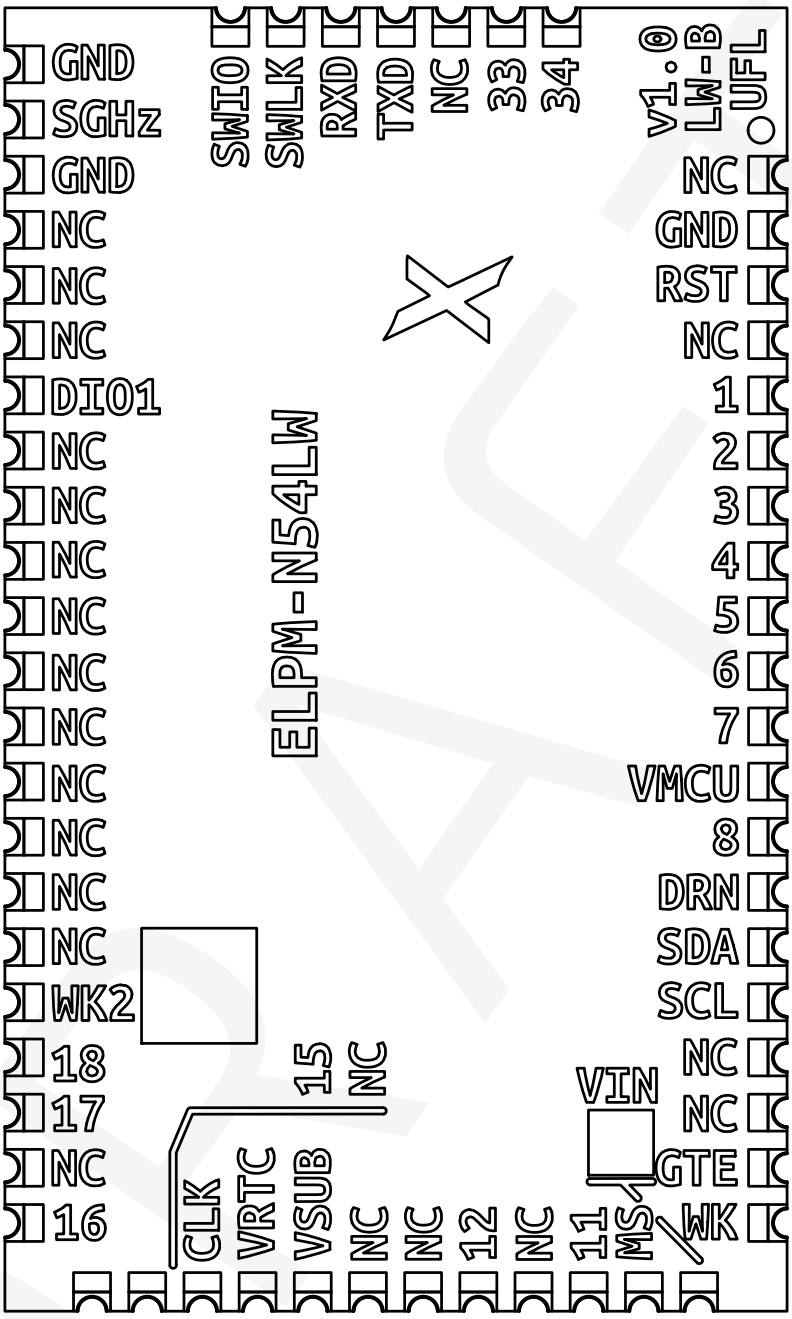


Figure 3.1: Pin names (bottom view)

3.1 | Pin Overview

The module has 62 castellated pins (1 to 60, plus A1 and A2). This table is derived from the rev1.0 PCB netlist and reports the actual nRF54L15 connections. Pins marked NC are physically present but are not electrically connected on this variant.

ELPM-N54LW and ELPM-S3LW use the same mechanical footprint and castellated-pin numbering. The common carrier-board interface includes GND, RESET, VMCU, VIN, PLATCH_DRAIN, PLATCH_GATE, PLATCH_WAKE, PLATCH_MASTER, SDA, SCL, VSUB, VRTC, RTC_CLK, WAKE2, LORA_DIO1 and SUB_GHz; pins 55 and 56 also retain RXD and TXD roles. A carrier board restricted to these common interfaces can accommodate either module when the supply, current and logic-level requirements

of the installed variant are satisfied. MCU-specific GPIO assignments, A1 RF connectivity, NC pins, optional power pins and firmware are variant dependent and shall be reviewed before substitution.

No.	Name	Type	ELPM-N54LW function
A1	NC	NC	Not connected on ELPM-N54LW rev1.0
A2	SUB_GHz	RF	SX1262 revB antenna, 50 Ω
1	GND	P	Ground
2	RESET	I	Active-low module reset input through the on-board nRF54L15 reset circuit
3	NC	NC	Not connected on ELPM-N54LW
4	P2.06	I/O	General-purpose I/O
5	P2.09	I/O	General-purpose I/O
6	P1.07	I/O	AIN3 / TAMPC
7	P1.08	I/O	CLK16M / TAMPC
8	P1.14	I/O	AIN7
9	P0.03	I/O	GRTC_PWMOUT
10	P1.11	I/O	AIN4
11	VMCU	P	Direct supply input for the nRF54L15 and ATECC608C rail
12	P1.12	I/O	AIN5
13	PLATCH_DRAIN	P	Switched power-latch output; tied to VMCU on N54LW rev1.0
14	SDA/GPIO	I/O	I²C SDA; P0.04 / GRTC_CLKOUT32K
15	SCL/GPIO	I/O	I²C SCL; P0.02
16	NC	NC	Not connected on ELPM-N54LW
17	NC	NC	Not connected on ELPM-N54LW
18	PLATCH_GATE	I/O	External MOSFET gate control; pull low externally to force power on
19	PLATCH_WAKE	I	Power-latch wake input
20	VIN	P	Direct power-latch input; externally regulated supply required
21	PLATCH_MASTER	I	Power-latch master input
22	P1.13	I/O	AIN6
23	NC	NC	Not connected on ELPM-N54LW
24	P1.09	I/O	TAMPC
25	NC	NC	Not connected
26	NC	NC	Not connected
27	VSUB	P	SX1262 direct supply rail
28	VRTC	P	RV-3028-C7 supply
29	RTC_CLK	O	RTC clock output
30	NC	NC	Not connected on ELPM-N54LW
31	P2.03/LED	O	On-board red status LED control
32	P1.10	I/O	TAMPC
33	NC	NC	Not connected on ELPM-N54LW
34	P1.02/NFC1	I/O	GPIO or NFC antenna terminal
35	P1.03/NFC2	I/O	GPIO or NFC antenna terminal

No.	Name	Type	ELPM-N54LW function
36	WAKE2 (RTC_EVI)	I	RTC event/wake input
37--46	NC	NC	Not connected on ELPM-N54LW
47	LORA_DIO1	I/O	SX1262 DIO1 and nRF54L15 P0.00
48--50	NC	NC	Not connected on ELPM-N54LW
51	GND	P	Ground
52	GND	P	Ground
53	SWDIO	I/O	Serial-wire debug data
54	SWDCLK	I	Serial-wire debug clock
55	P1.05/RXD	I/O	AIN1 / TAMPC; UART assignment is configurable
56	P1.04/TXD	I/O	AIN0 / TAMPC; UART assignment is configurable
57	NC	NC	Not connected
58	P2.08	I/O	General-purpose I/O
59	P2.10	I/O	General-purpose I/O
60	GND	P	Ground

Type legend: I=input, O=output, I/O=bidirectional, P=power, RF=radio-frequency interface, NC=not connected. Peripheral functions and drive capabilities depend on the selected nRF54L15 configuration.

Two auxiliary contacts are provided on the underside of the module. AUX-VIN is electrically connected to VIN and follows the same voltage limits and power-latch behaviour. AUX-GND is electrically connected to ground. These contacts are intended for wiring, prototyping and test access and are not required in the recommended castellated host footprint.

3.2 | Pins used internally

- I²C peripherals: SDA=P0.04, SCL=P0.02
- Power-latch hold: AUTO TURN OFF=P2.07
- Battery level: P1.06/AIN2
- Status LED: P2.03
- SX1262: P2.00 (RST), P2.01 (SCK), P2.02 (MOSI), P2.04 (MISO), P2.05 (NSS), P0.01 (BUSY), P0.00 (DIO1)

The I²C bus remains available on pins 14 and 15 and includes on-board 10 kΩ pull-up resistors to VMCU. Do not drive either line above VMCU or while VMCU is unpowered unless suitable isolation prevents back-powering.

4 | Electrical characteristics

4.1 | Absolute maximum ratings

Stresses beyond the specified limits may cause permanent damage to the module. These are stress ratings only; functional operation at these limits is not implied. Because VIN is passed to the main rail without voltage conversion, it must never be treated as a 5 V-tolerant supply input.

Symbol	Parameter	Min	Max	Unit
VMCU	Main nRF54L15/ATECC608C rail	-0.3	3.9	V
VIN	Power-latch input; propagated to VMCU when on	-0.3	3.9	V
VSUB	SX1262 VBAT and VBAT_IO rail	-0.5	3.9	V
VRTC	RV-3028-C7 supply pin	-0.3	6.0	V
VIO	Exposed nRF54L15 GPIO voltage	-0.3	VMCU+0.3[a]	V
I_{DRAIN}	PLATCH_DRAIN path current	-	1	A

[a]Not to exceed 3.9 V. VRTC signals must also remain between -0.3 V and VRTC+0.3 V. The 1 A DRAIN value is an absolute path limit, not a recommended continuous-current rating. The application shall remain within the recommended operating conditions below and provide suitable margin.

4.2 | Recommended operating conditions

To ensure the proper operation of the ELPM-N54LW, the following ranges must be observed.

Symbol	Parameter	Min	Max	Unit
VMCU	Direct nRF54L15 and ATECC608C supply rail	2.0	3.6	V
VIN	Direct power-latch input; switched onto the main rail without regulation	2.0	3.6	V
VSUB	Direct supply rail for the SX1262	1.8	3.7	V
VRTC	RV-3028-C7 rail in the recommended shared-voltage configuration	2.0	3.6	V

VIN passes through the power latch without voltage conversion, while VMCU bypasses the latch and directly supplies the main rail. VSUB directly supplies both VBAT and VBAT_IO of the SX1262. A battery or source outside the applicable rail range requires an external regulator.

The nRF54L15 itself supports a 1.7--3.6 V supply and contains a single-inductor DC/DC converter. The module-level VMCU and VIN minimum is 2.0 V because the ATECC608C on the same rail requires at least 2.0 V. The nRF54L15 DC/DC converter regulates only the SoC internal domains; it does not generate a regulated output for other module circuits or external loads.

Supplying VRTC and VMCU from the same source is the recommended configuration. The RV-3028-C7 component supports 1.1--5.5 V for timekeeping and 1.2--5.5 V for 100 kHz I²C, but its input-high threshold is 0.8×VRTC. The on-module I²C pull-ups are connected to VMCU, while WAKE2/EVI and RTC_CLK are referenced to VRTC. If different sources are used, VMCU must be at least 0.8×VRTC for a pulled-up I²C high level to be recognized, and every connected signal must remain within the absolute pin-voltage limits of both domains. External level adaptation is required when these conditions cannot be guaranteed, including during power transitions.

The SX1262 has no level shifter between its VSUB-referenced digital interface and the VMCU-referenced nRF54L15 GPIOs. Supplying VSUB and VMCU from the same regulated source is therefore recommended. With separate sources, all of the following worst-case conditions must be satisfied: VMCU-0.4 V $\geq$ 0.7×VSUB for signals driven by the nRF54L15; 0.9×VSUB $\geq$ 0.7×VMCU for signals driven by the SX1262; and |VMCU-VSUB| $\leq$ 0.3 V to remain within the absolute I/O limits. These conditions must hold during startup, shutdown and steady-state operation.

4.3 | Maximum ESD ratings

Module-level ESD immunity is under characterization. No IEC 61000-4-2 system-level rating is claimed in this revision. Most exposed GPIO and control pins connect directly to on-module ICs or logic and do not include dedicated system-level ESD protection.

The SUB_GHz antenna path includes a low-capacitance RF protection device rated at component level for ±14 kV contact discharge and ±18 kV air discharge according to IEC 61000-4-2. These values characterize the protection component only and are not an immunity rating for the complete ELPM-N54LW. External protection must be selected by the integrator according to the accessible interfaces and compliance requirements of the final product.

The VMCU rail also includes an on-module transient-protection device. The protection component is rated for ±12 kV contact discharge and ±15 kV air discharge according to IEC 61000-4-2. These are component-level values and do not constitute an ESD immunity rating for the VMCU rail or for the complete module.

4.4 | Operating temperature range

Parameter	Min	Max	Unit
Operating temperature	-40	+85	°C

4.5 | GPIO DC characteristics

Digital I/O levels of the exposed GPIOs, from the nRF54L15 product specification:

Symbol	Parameter	Min	Max	Unit
VIH	High-level input voltage	0.7×VDD	VDD	V
VIL	Low-level input voltage	VSS	0.3×VDD	V
VOH	High-level output voltage, standard drive, 0.5 mA	VDD-0.4	VDD	V
VOL	Low-level output voltage, standard drive, 0.5 mA	VSS	VSS+0.4	V

5 | RF characteristics

The module provides two independent 50 Ω antenna interfaces through U.FL connectors, identified as GHz and SUB_GHz. External antennas are required and are not included with the module. Values in this section are component-level references; module-level conducted and radiated performance remains subject to N54LW characterization.

5.1 | Antenna interfaces

Connector	Radio	Impedance
GHz	nRF54L15 multiprotocol 2.4 GHz radio	50 Ω
SUB_GHz	SX1262 revB Sub-GHz radio	50 Ω

5.2 | GHz radio

The integrated nRF54L15 supports Bluetooth LE, Bluetooth Mesh, Bluetooth Channel Sounding, IEEE 802.15.4 for Thread, Zigbee and Matter, and proprietary 2.4 GHz operation up to 4 Mbps.

For component-level RF performance, output-power settings, sensitivity and protocol-dependent limits, refer to the official nRF54L15 product specification. Component current references are reported separately in Section 6.2.

5.3 | Sub-GHz radio (SUB_GHz)

The populated revB radio path uses the SX1262. The following component-level values require module-level confirmation:

Parameter	Condition	Value
Frequency range	Design target	862 MHz to 928 MHz
TX output power	Configurable	-9 dBm to +22 dBm
LoRa spreading factor	-	SF5 to SF12
LoRa bandwidth	-	7.8 kHz to 500 kHz
LoRa air data rate	-	up to 62.5 kbps
(G)FSK air data rate	-	0.6 kbps to 300 kbps
Sensitivity	LoRa, SF12, BW 10.4 kHz	-148 dBm
Sensitivity	LoRa, SF12, BW 125 kHz	-137 dBm
Sensitivity	LoRa, SF7, BW 125 kHz	-124 dBm
TX current	+22 dBm	118 mA typ
RX current	LoRa, BW 125 kHz	4.6 mA typ

5.4 | Antenna requirements

Both interfaces require 50 Ω antennas. Antenna gain and feed losses must be included when checking the ERP/EIRP limits of the target region. Final-product certification remains the integrator's responsibility.

6 | Power management

The ELPM-N54LW integrates an external power-latch architecture. Deep Stop removes power from the main MCU domain and complements the native nRF54L15 System OFF and sleep modes.

When the module is supplied through VIN, the power latch switches the external voltage directly onto the VMCU rail for the nRF54L15 and ATECC608C. The source connected to VIN must therefore already be regulated within the 2.0--3.6 V module range. VMCU is a direct alternative supply input and bypasses the latch.

The nRF54L15 integrates its own single-inductor DC/DC converter for the SoC internal domains and accepts 1.7--3.6 V at device level. This internal converter does not regulate the VMCU rail. The 2.0 V module-level minimum is imposed by the ATECC608C sharing that rail.

For local VMCU decoupling, 10 μF and 1 μF capacitors in parallel are recommended close to the module pin. A local bulk capacitor at VIN is also recommended when the supply connection is long or the source has appreciable impedance. Final mandatory capacitance requirements are subject to module-level validation.

6.1 | Supply configurations

The power pins support the following supply configurations. MCU-domain and radio-domain configurations may be combined where the stated voltage and logic-level requirements are satisfied.

Configuration	Connections	Pins left floating
Power-latch supply	Apply externally regulated 2.0--3.6 V to VIN	Leave VMCU un-driven
Direct main-rail supply	Apply externally regulated 2.0--3.6 V to VMCU	Leave VIN floating
Direct Sub-GHz supply	Apply 1.8--3.7 V directly to VSUB	Leave unused NC pins floating

VRTC and VSUB are dedicated supply inputs and shall not be used as power outputs. Supplying VRTC, VSUB and VMCU from the same compatible regulated source is the recommended configuration. VRTC may remain supplied while the main rail is off so that the RTC can retain time and wake the power latch. VSUB may remain supplied for packet wake-up, or may be switched with the main rail when an external source is routed accordingly. Separate rail voltages are permitted only when the logic-level and absolute pin-voltage conditions in Section 4 remain satisfied throughout power transitions. Pins 23, 30 and 33 are not connected on ELPM-N54LW.

The configurations are detailed below:

- **Power-latch mode:** apply an externally regulated 2.0--3.6 V supply to VIN. The latch switches that voltage directly onto the nRF54L15 and ATECC608C rail. Do not drive VMCU from a second source in this configuration.
- **Direct MCU supply:** apply an externally regulated 2.0--3.6 V supply to VMCU and leave VIN floating. This bypasses the power-latch path and directly supplies the nRF54L15 and ATECC608C rail.
- **RTC wake source:** normally connect VRTC to the same compatible source as VMCU. VRTC may instead remain supplied while the main power latch is off so that a programmed RTC timer/alarm or an external event on WAKE2/EVI can assert the RTC interrupt connected to the power-latch wake path. The module has no internal RTC backup battery, so removing VRTC stops timekeeping and loses the stored date and time. A separate VRTC source must satisfy the interface conditions in Section 4.
- **Direct Sub-GHz supply:** apply 1.8--3.7 V to VSUB. Using the same compatible regulator for VSUB and VMCU is recommended, and the source must supply the SX1262 peak current. Separate sources require the SPI logic-level and absolute pin-voltage conditions in Section 4 to remain valid in every operating and power-transition state.

PLATCH_DRAIN is an unregulated switched copy of VIN. When the power latch is active, its voltage is nominally equal to VIN apart from the small voltage drop of the internal path; it must not be treated as a precision regulated supply. The internal switching implementation is not part of the module interface specification.

PLATCH_DRAIN may supply an external load that must follow the module power state. For additional or substantial load current, use an external MOSFET controlled by PLATCH_GATE instead of routing the load current through PLATCH_DRAIN. The 1 A value stated in the absolute maximum ratings is not a recommended continuous-load rating.

When the power latch is off, PLATCH_DRAIN is high-impedance and is not actively discharged. Its decay time therefore depends on the connected load and external capacitance. Applications requiring a defined or rapid discharge shall provide a suitable external discharge path.

PLATCH_GATE exposes the latch control node. Its primary function is to control the gate of an external MOSFET, allowing additional loads to turn on and off together with the module power latch. The same node can also be used as an input: pulling it low externally forces the power latch on. External circuitry connected to this node must not drive it high against the internal latch state.

6.2 | Power consumption

The Deep Stop values below are reference values for the power-latch and RTC circuitry and require confirmation on N54LW engineering samples. Values identified as component data are taken from the respective manufacturer datasheets under the stated conditions; they do not include the complete module or external loads and are not production-tested module limits.

Work mode	Description	Temp	Vin	Min	Typ	Unit
Deep Stop (RTC disabled)	MASTER, GATE or WAKE input triggering the power latch. RTC not powered.	+20°C to +30°C	3.3V	<1	5	nA
Deep Stop with RTC	RTC powered. Multiple interrupt sources.	+20°C to +30°C	3.3V	40	80	nA
System OFF[a]	nRF54L15, wake on pin, 0 kB RAM retention.	+25°C	3.0V	-	0.7	µA
System ON idle[a]	nRF54L15, wake on pin, 0 kB RAM retention.	+25°C	3.0V	-	0.8	µA
2.4 GHz RX[a]	nRF54L15 radio only, Bluetooth LE 1 Mbit/s.	+25°C	3.0V	-	2.1	mA
2.4 GHz TX[a]	nRF54L15 radio only, 0 dBm.	+25°C	3.0V	-	3.7	mA
2.4 GHz TX max[a]	nRF54L15 radio only, maximum QFN power setting.	+25°C	3.0V	-	9.1	mA
Sub-GHz TX[b]	SX1262 transmitting @ +22 dBm.	+25°C	3.3V	-	118	mA
Sub-GHz RX[b]	SX1262 receiving (LoRa, BW 125 kHz).	+25°C	3.3V	-	4.6	mA

[a] Values measured and published by Nordic for the nRF54L15 component; radio values are radio-only figures. Nordic specifies the TX current by output-power setting and publishes the RX value for Bluetooth LE modes, but does not publish a distinct, directly comparable IEEE 802.15.4 RX/TX current in the nRF54L15 radio-current tables. Actual current depends on radio mode, DC/DC configuration, enabled peripherals, memory retention, firmware and temperature. [b] SX1262 contribution only; add the nRF54L15 current of the selected work mode. Component-reference values are not substitutes for a complete module power budget.

6.3 | Auto turn off (power latch control)

Only when the system is supplied from VIN through the power latch, firmware controls shutdown through AUTO TURN OFF on nRF54L15 P2.07. Configure P2.07 as an output and drive it high as

one of the first firmware operations. Keep it high for the complete powered phase and drive it low only to request shutdown. The maximum allowed startup delay requires N54LW characterization. While AUTO TURN OFF is held high, it forces the power latch to remain on and subsequent events on MASTER, WAKE or GATE are ignored. These inputs become effective again after the controlled shutdown has released the latch.

When the module is supplied directly through VMCU, the power-latch path is bypassed and P2.07 does not control the external VMCU source.

6.4 | Sub-GHz packet wake-up

The exposed LORA_DIO1 pin may be connected externally to PLATCH_MASTER to turn on the power latch when the SX1262 asserts DIO1, for example after a valid packet reception. This configuration has been functionally verified on engineering hardware. The radio must be configured before shutdown so that the required IRQ is routed to DIO1, and the SX1262 supply, including its VBAT_IO domain, must remain active while waiting for the event. After startup, AUTO TURN OFF is held high and forces the latch on; consequently, the opposite MASTER edge produced when firmware clears the radio IRQ and DIO1 returns inactive is ignored and does not disturb the powered state.

Before turning the nRF54L15 off, firmware should configure the connected SPI and control GPIOs as inputs with internal pulls disabled whenever permitted by the radio state. This reduces actively driven paths during shutdown but does not provide galvanic isolation: after VMCU is removed, the nRF54L15 no longer retains the software GPIO configuration and an active SX1262 output may inject current through an unpowered nRF54L15 pad. Consequently, this packet-wake configuration does not carry the nanoampere Deep Stop current specification; its total off-state current includes the selected SX1262 receive mode and any residual interface current. Hardware isolation is required when guaranteed elimination of interface back-powering is needed.

6.5 | Startup time

The complete N54LW startup time depends on the selected trigger, nRF54L15 boot configuration and firmware. MASTER, WAKE and scheduled RTC startup shall be characterized on assembled modules.

Interrupt mode	Description	Typ	Unit
MASTER P.Latch	Change of input status.	TBD	ms
RTC WAKE	Scheduled wake-up.	TBD	ms
WAKE	WAKE input to GND.	TBD	ms

6.6 | Deep Stop performance

New Otii captures are required for MASTER, WAKE and RTC cycles using the N54LW hardware and firmware. Until those measurements are complete, no current-consumption traces are published.

7 | On-board peripherals

The module integrates the RTC and secure element on the same I²C bus (SDA: P0.04, SCL: P0.02), with integrated 10 kΩ pull-up resistors to VMCU, together with a status LED and the battery-level circuit. The bus is deliberately routed through GPIO port P0, which belongs to the nRF54L15 low-power domain. This allows the low-power-domain I²C peripheral to be used without keeping the power domains associated with P1 and P2 active, when permitted by the selected firmware and application configuration.

7.1 | I²C address map

Device	Function	I²C address
RV-3028-C7	Real time clock	0x52
ATECC608C	Secure element	0x60

The on-board pull-up resistors are referenced to VMCU. External devices on this bus must not drive SDA or SCL above VMCU or while VMCU is unpowered, unless suitable isolation is provided to prevent back-powering.

7.2 | RTC (RV-3028-C7)

Extreme low power external real time clock (45 nA to 100 nA), used by the Deep Stop mode for scheduled or event-driven wake-up. It features a dedicated power supply pad (VRTC), a clock output (RTC_CLK pin) and an external event input (WAKE2, connected to the RV-3028-C7 EVI pin).

When VRTC is supplied, the RTC can assert its interrupt output either from an internally programmed timer/alarm or from an event detected on WAKE2/EVI. The RTC interrupt is connected internally to the wake path of the power latch. For example, a one-minute periodic timer produces one interrupt and one system startup every minute. Alternatively, WAKE2 allows an external signal to use the same RTC interrupt path and may also use the RTC event-detection and time-stamp functions. WAKE2 includes an on-module 10 kΩ pull-down resistor and does not require an external resistor to define its inactive state. Configure the RTC event input for an active-high level or rising-edge event; active-low operation is not supported as a module configuration because the pull-down defines low as the normal inactive state. Do not drive WAKE2 above VRTC or while VRTC is unpowered. WAKE2-based wake-up is unavailable when VRTC is not powered. Event filtering, interrupt routing and flag clearing must be configured through the RTC registers as described in the RV-3028-C7 application manual.

The ELPM-N54LW does not include an internal backup battery for the RTC. VRTC must remain externally supplied to preserve timekeeping while the main system is off; removing VRTC stops the RTC and the stored date and time are lost.

Connecting VRTC to VMCU is recommended. The on-board I²C pull-ups are tied to VMCU, while the RTC input thresholds depend on VRTC; consequently, supplying the RTC above the specified module VRTC range requires suitable level adaptation for I²C and the other RTC-domain signals.

7.3 | Secure element (ATECC608C)

The ATECC608C is a secure element providing hardware-based secure key storage and cryptographic acceleration: ECDSA sign/verify and ECDH key agreement on the ECC P-256 curve, SHA-256, AES-128 and monotonic counters. The module mounts the standard I²C version of the device, shipped unprovisioned: all key slots are free, no slot is occupied or reserved by OBJEX, and both the Configuration Zone and Data Zone are supplied unlocked and fully available for the end user. When the secure element is correctly configured and locked, private keys generated in non-readable slots remain inside the device and cryptographic operations involving them are executed in hardware. Provisioning, access policies and configuration locking are the responsibility of the end user.

7.3.1 | Module authenticity

During provisioning the end user can give each module a unique cryptographic identity: a device certificate whose private key is generated and locked inside the secure element. The infrastructure can then verify possession of that identity through a challenge-response mechanism: the module signs a random challenge with its private key and the verifier checks the signature against the device certificate chain. This authenticates the provisioned device identity; system-level tamper resistance depends on the complete product design and provisioning process.

7.3.2 | Example: MQTT with mutual TLS

An MQTT broker can be configured to require mutual TLS (mTLS): the module authenticates itself during the TLS handshake by signing with the private key stored in the ATECC608C, and access to specific topics can be restricted to authenticated clients only. Since the private key cannot be extracted or duplicated, the client identity cannot be forged.

7.3.3 | Sub-GHz security layer

The secure element also benefits the sub-GHz radio. For LoRaWAN the user can store the root keys in the device and use it to compute the AES-CMAC message integrity code. For proprietary sub-GHz protocols, transmitted messages can be signed (ECDSA) or authenticated (AES-CMAC), guaranteeing the authenticity and integrity of every frame and protecting the network from spoofing and tampering; monotonic counters can be used to prevent replay attacks.

7.3.4 | Regulatory context

The hardware root of trust provided by the secure element (unique device identity, protected key storage, verification of update authenticity) gives the final product a solid hardware foundation to meet the essential cybersecurity requirements of the EU Cyber Resilience Act (Regulation (EU) 2024/2847).

7.4 | Status LED

The on-board red status LED is driven directly by nRF54L15 P2.03 through a 220 Ω current-limiting resistor. The LED is active high: drive P2.03 high to turn it on and low to turn it off. The LED circuit operates from 1.8 V; the complete module must nevertheless remain within the recommended VMCU operating range specified in Section 4.

7.5 | Battery level

The battery-level input is connected to nRF54L15 P1.06/AIN2 through a resistive divider made of two 100 kΩ resistors. The divider ratio is 1:2, therefore the nominal ADC voltage is half the battery voltage:

$$V_{\mathrm{AIN2}} = \frac{V_{\mathrm{BAT}}}{2}.$$

The divider presents a nominal 50 kΩ Thevenin source resistance to the ADC and draws $V_{\mathrm{BAT}}/200\,\mathrm{k\Omega}$ from the monitored supply. ADC acquisition time, attenuation and calibration shall be selected accordingly.

8 | Software support

The ELPM-N54LW is supported through the Nordic nRF Connect SDK and Zephyr RTOS development ecosystem. Applications can use the drivers, protocol stacks, power-management facilities and security features available for the nRF54L15, together with the module-specific peripheral interfaces.

Engineering samples are shipped with a basic red status LED blink firmware for functional indication. When the module is supplied through VIN, this firmware asserts AUTO TURN OFF so that the power latch remains on. The test firmware is not locked, may be completely replaced by the user and will be published through the official repository.

Ready-to-use firmware examples are published and maintained through the official OBJEX Labs repository:

github.com/OBJEX-Labs/OBJEX_ELPMs

Available examples cover:

- Red status LED blink
- Power latch with MASTER/WAKE inputs and AUTO TURN OFF
- RTC scheduled wake-up
- LoRa point-to-point ping-pong

LoRa point-to-point is the most extensively tested radio example. A LoRaWAN example is not listed as available in this revision because it has not yet been validated on ELPM-N54LW.

The examples are provided as a convenience layer and do not constrain the application architecture. The purchaser retains full control of the nRF54L15 firmware and may replace or modify the application, boot chain, update mechanism, protocol stacks and peripheral configuration using the facilities supported by the selected nRF Connect SDK release. The module is not shipped with a user-locked application framework.

8.1 | Power-latch startup requirement

When the module starts from VIN through the power latch, firmware must configure nRF54L15 P2.07 (AUTO TURN OFF) as an output and drive it high as one of the first operations. Keep it high while the system must remain powered and drive it low only for controlled shutdown. The maximum permitted assertion delay requires N54LW measurement. This requirement does not apply when VMCU is supplied directly.

8.2 | Programming and debugging interfaces

The on-board reset circuit keeps RESET in its inactive state, so the nRF54L15 starts normally when power is applied without requiring external reset components. RESET remains available on module pin 2 for manual reset and programming control.

Program and debug the nRF54L15 through SWDIO (module pin 53), SWDCLK (module pin 54), RESET (module pin 2), VMCU and GND. Engineering samples are supplied without debug protection enabled, leaving SWD accessible to the user. Use tools supported by the nRF Connect SDK, such as a compatible SEGGER J-Link probe. Pins 55 and 56 are routed to P1.05 and P1.04 and may be configured as UART RX/TX in firmware; they do not implement a fixed ROM serial-download interface.

The nRF54L15 does not expose native USB on module pins 25 and 26; those common-socket pins are not connected on ELPM-N54LW rev1.0.

9 | Typical applications

The following reference schematics show typical supply configurations of the ELPM-N54LW. Ready-to-use KiCad projects will be published through the official OBJEX Labs ELPM repository after validation against the released module revision.

9.1 | Direct constant supply

Apply an externally regulated 2.0--3.6 V supply to VMCU and leave VIN floating. This directly supplies the nRF54L15 and ATECC608C and bypasses the power-latch path.

To power the Sub-GHz radio from the same external source, connect VMCU and VSUB to that source only when its voltage is within both permitted ranges and it can provide the SX1262 peak current. If the Sub-GHz radio is not required, leave VSUB unpowered.

VRTC may also be connected to a compatible source when RTC operation is required.

Reference design: direct constant supply.

9.2 | Battery supply with power latch and external wake source

Battery powered through the power latch: an external source triggers a power-latch input and turns the system on only when an event occurs. The source may be a sensor, a switch, a logic output or any other circuit that produces the required voltage transition. MASTER reacts to either change of input state, while WAKE follows its specified active level. PLATCH_GATE normally controls an external MOSFET but may also be pulled low externally to force the latch on.

If the Sub-GHz radio must follow the same switched power state, route the switched rail externally to VSUB, provided its voltage is valid for the SX1262. To keep the radio powered independently, supply VSUB from a separate compatible source.

Reference design: battery power latch with external wake source.

9.3 | Battery supply with power latch and periodic RTC wake-up

Battery powered through the power latch: a sensor (for example a temperature sensor) is switched off together with the system and read at each periodic wake-up scheduled by the RTC. VRTC must remain supplied while the main system is off. The same wake path may instead be activated by an external event connected to WAKE2/EVI, after enabling and configuring the RTC event interrupt.

Reference design: RTC periodic wake-up sensor node.

9.4 | Sub-GHz packet wake-up

Keep the SX1262 supply active and connect the exposed LORA_DIO1 pin to PLATCH_MASTER. When the radio is configured to route a packet-reception IRQ to DIO1, the DIO1 transition activates the power latch and starts the nRF54L15. This mode keeps the radio and its I/O supply active and therefore has a higher off-state current than Deep Stop with the radio disabled; see Section 6.4.

Reference design: Sub-GHz packet wake-up.

10 | Design guidelines

10.1 | Module placement and layout

- Follow the recommended PCB footprint (Section 11.4).
- Do not route signal traces or place vias on the top layer of the host board under the module body: keep the area limited to the footprint pads and to a solid ground pour.
- Connect the castellated GND pins to a solid ground plane. The auxiliary bottom VIN and GND contacts are optional and are primarily intended for point-to-point or minimal-carrier assemblies.
- Leave enough clearance around the castellated edges for soldering inspection and rework.
- Keep the area around the two U.FL receptacles clear, so that the coaxial plugs can be mated and the cables routed without stress.

The RF shield can is electrically connected to module GND. Do not use the shield can as a power or signal connection, and prevent conductive mechanical parts from applying unintended current through it.

10.2 | Antenna connections

Both RF interfaces use the same standard U.FL coaxial receptacle (50 Ω) soldered on the module. To connect the antennas, use 50 Ω cable assemblies terminated with a standard U.FL mating plug (Hirose U.FL-LP series or compatible). Note that this connector family is rated for a limited number of mating cycles (typically 30): use the dedicated extraction tool and avoid unnecessary connect/disconnect cycles.

10.3 | External circuitry

- SWD: protect and route SWDIO/SWDCLK according to accessibility and production-test requirements; pins 25/26 are not connected on N54LW rev1.0.
- Exposed signals: add application-appropriate ESD protection to GPIOs, control inputs and other interfaces that are accessible in the final product.
- WAKE/MASTER inputs: keep their levels within the applicable module supply domain, drive them through a high value resistance to GND (never floating), and keep the traces short to avoid spurious wake-up events.
- WAKE2/EVI: an on-module 10 kΩ pull-down defines the inactive state. Configure the RTC for an active-high level or rising-edge event. Keep the applied level within the VRTC domain and do not drive the pin while VRTC is unpowered.
- Power input: place a local bulk capacitor close to the VIN pin when the supply cable is long or the battery has a high internal resistance.
- PLATCH_DRAIN loads: the 1 A value is an absolute maximum for the switched path, not a recommended continuous operating current. Design external loads with significant current and thermal margin.
- VMCU decoupling: place 10 μF and 1 μF capacitors in parallel close to the VMCU pin, using short connections to the ground plane.
- Separate VMCU and Sub-GHz supplies: ensure that the SPI input levels remain valid for both devices during normal operation, startup and shutdown. Prevent an active SPI signal from unintentionally powering an unpowered rail through an I/O pin.
- Optional supply domains: VRTC and VSUB are inputs only and shall not supply external loads. Leave every pin identified as NC in the pin table electrically unconnected.

10.4 | Configurable host-board power routing

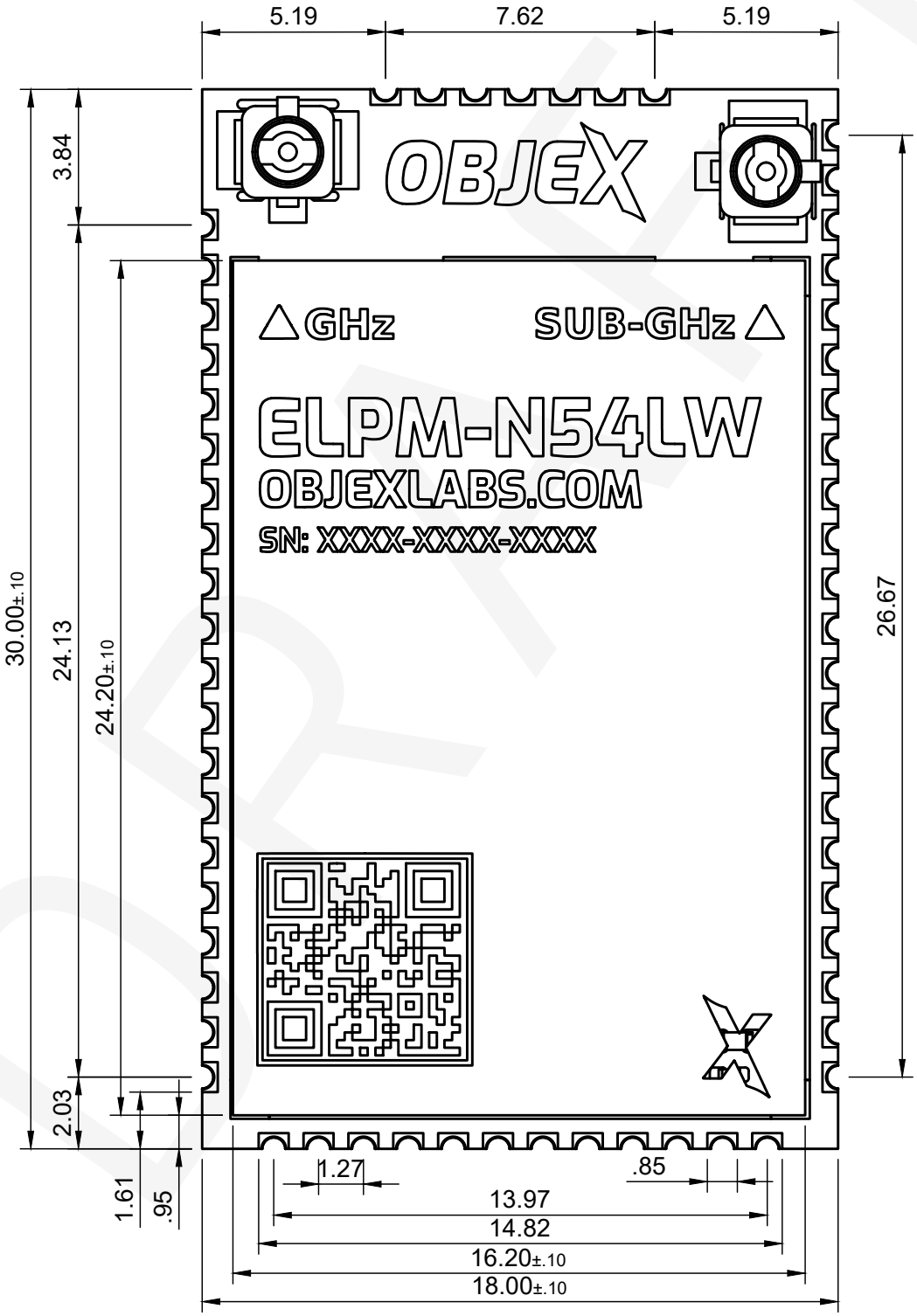
For prototypes, test fixtures and host boards intended to support multiple power configurations, optional individually populated 0 Ω links are recommended on the VRTC and VSUB source paths. They allow individual domains to be disconnected during debugging, current measurement and fault isolation, and let one PCB layout select an always-on or switched RTC and an always-on, power-latch-controlled or independently regulated Sub-GHz radio. These links are a design and test convenience, not a mandatory requirement for a fixed production configuration.

Place the links so that each supply path can be inspected and reconfigured independently. Do not connect independent sources simultaneously to VIN and VMCU. The voltage range and power-sequencing requirements of every selected configuration remain applicable.

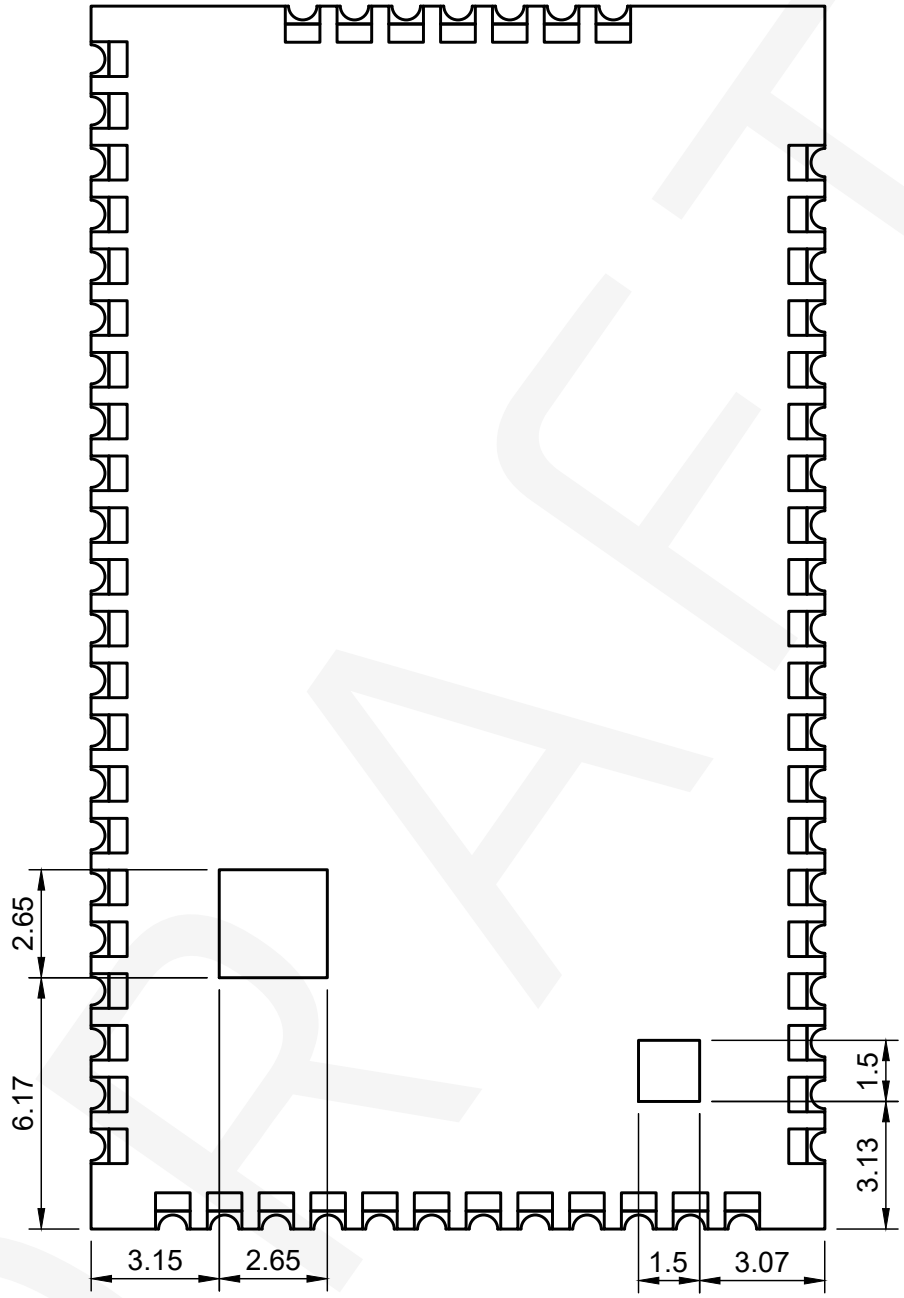
11 | Physical Dimensions

The nominal module outline is 18 mm × 30 mm, with a nominal overall height of 2.75 mm and a nominal module-base thickness of 0.71 mm. Dimensions in the drawings are expressed in millimeters; production tolerances remain subject to mechanical qualification.

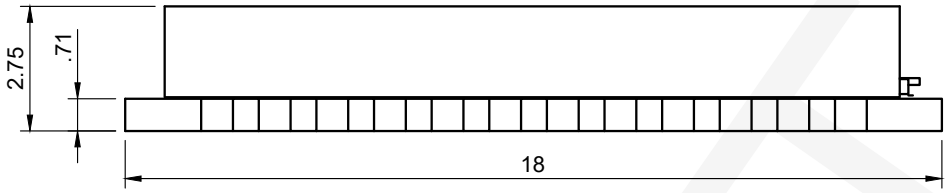
11.1 | Top view



11.2 | Bottom view



11.3 | Side view



11.4 | Recommended PCB footprint

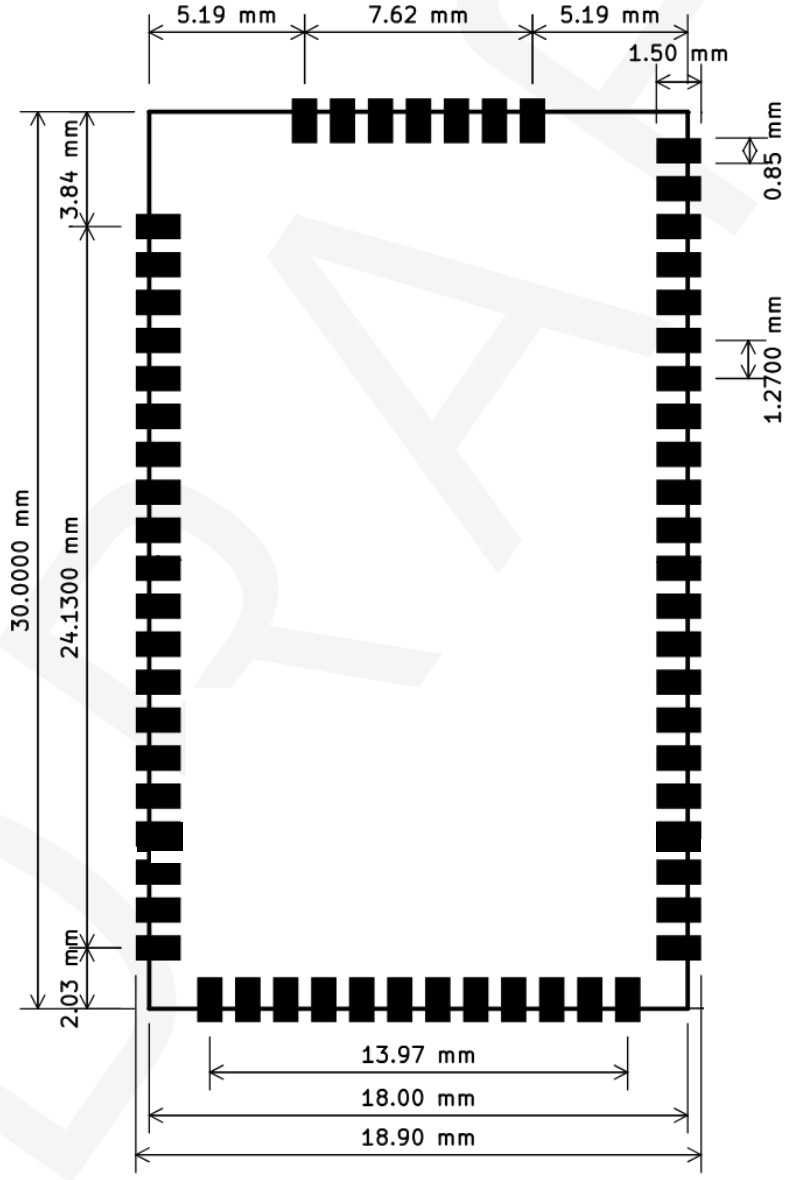


Figure 11.1: Recommended host-PCB footprint. Auxiliary underside VIN and GND contacts are intentionally omitted.

12 | Soldering and handling

12.1 | Reflow soldering

The module contains lead-free SAC-type internal solder joints with a liquidus temperature of approximately 217 °C. These joints shall not be allowed to reflow during host-board assembly. Use a low-temperature lead-free solder paste suitable for the host PCB and keep the temperature measured on the module below 217 °C throughout the complete process. A SnBi- or SnBiAg-based process is recommended.

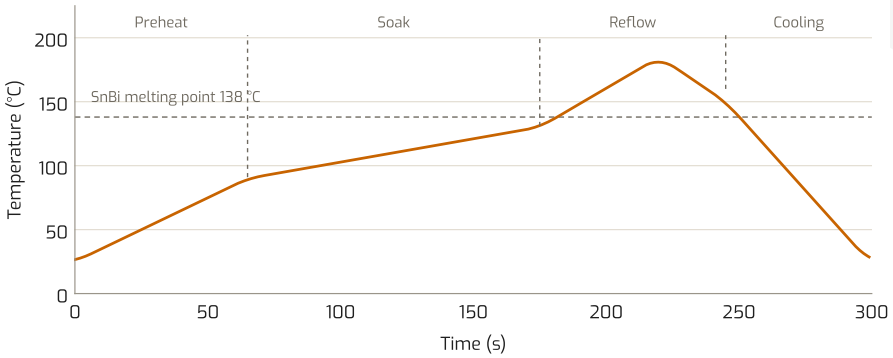


Figure 12.1: Recommended low-temperature reflow profile.

Profile parameter	Recommended value
Ramp-up rate	≤ 2 °C/s
Preheat/soak	60 s to 120 s, 90 °C to 130 °C
Peak temperature	170 °C to 190 °C
Time above paste liquidus	45 s to 90 s
Ramp-down rate	≤ 3 °C/s
Maximum reflow cycles	2

The values above are starting limits for process development, not a substitute for the selected solder-paste specification. Validate the profile on the actual host assembly using a thermocouple attached to the module, accounting for PCB size, copper distribution, component loading and oven characteristics. A conventional high-temperature SAC reflow profile is not supported for host-board assembly because it can reflow the module's internal joints. If the required joint quality cannot be achieved while respecting these limits, use a selective or hand-soldering process instead.

12.2 | Moisture sensitivity

Engineering samples have not been assigned a moisture sensitivity level. They are supplied in sealed ESD-protective bags; this packaging shall not be interpreted as qualified moisture-barrier packaging. Floor-life and baking conditions are not specified in this revision and will be defined only after module-level qualification according to J-STD-020 and handling-process validation according to J-STD-033.

12.3 | Storage conditions

Keep engineering samples in their sealed ESD-protective bags and store them in a dry, non-condensing environment, protected from corrosive atmospheres, direct sunlight and rapid temperature changes. No qualified temperature, humidity or shelf-life limit is assigned in this revision.

12.4 | ESD handling precautions

The module is an electrostatic discharge sensitive device. Handle it only at ESD-protected workstations (grounded wrist strap, dissipative surfaces) in accordance with IEC 61340-5-1 or ANSI/ESD S20.20, and keep it in its original protective packaging until assembly.

13 | Ordering information

Preliminary: order codes and packaging details will be finalized before mass production.

Order code	Description	Packaging
ELPM-N54LW-R10B	Revision 1.0, 868--925 MHz Sub-GHz band variant	Engineering samples: sealed ESD bag

Every engineering sample is functionally tested before shipment. The engineering-sample package contains the module only. External antennas, coaxial cables and other accessories are not included. The module is not currently available as a standard orderable production product.

13.1 | Product marking

Each engineering sample is marked on the top overlay with the product name, the manufacturer website and a unique serial number. The serial-number format is EGSE-NL26-Bxxx: EGSE identifies an engineering sample, NL identifies the N54LW module, 26 is the production year, B identifies the 868--925 MHz Sub-GHz band variant and the final characters form an incremental unit number. The QR code encodes exactly the same serial-number string, allowing fast identification and unit-level traceability.

14 | Certifications

Certification activities are in progress: internal verification is being completed before laboratory testing. The table below will be updated as the activities progress.

Certification	Region	Status
CE (RED)	Europe	In progress

14.1 | Material compliance (RoHS, REACH)

The module is designed and manufactured to comply with Directive 2011/65/EU (RoHS 2) as amended by Directive (EU) 2015/863, and with Regulation (EC) 1907/2006 (REACH). Compliance declarations will be made available together with the product certifications.

14.2 | WEEE (RAEE)

In accordance with Directive 2012/19/EU on waste electrical and electronic equipment (WEEE, implemented in Italy as RAEE), this product must not be disposed of with unsorted municipal waste at the end of its life. The crossed-out wheeled bin symbol indicates that the product is subject to separate collection: return it to an authorized collection point or to the distributor for proper treatment, recovery and recycling.

15 | Related documentation

- nRF54L15 Product Specification - Microcontroller and 2.4 GHz radio
- nRF54L15 product page - Documentation, software and reference designs
- nRF Connect SDK - Software development platform
- Zephyr Project documentation - RTOS and application framework
- SX1262 - Sub-GHz radio IC
- RV-3028-C7 - Extreme low power ext. RTC
- ATECC608C - Secure element

16 | Acronyms

- **ADC** - Analog to Digital Converter
- **BLE** - Bluetooth Low Energy
- **SWD** - Serial Wire Debug
- **EIRP** - Effective Isotropic Radiated Power
- **ERP** - Effective Radiated Power
- **ESD** - Electrostatic Discharge
- **(G)FSK** - (Gaussian) Frequency Shift Keying
- **GPIO** - General Purpose Input/Output
- **MSL** - Moisture Sensitivity Level
- **mTLS** - mutual Transport Layer Security
- **NC** - Not Connected
- **RTC** - Real Time Clock
- **SF** - Spreading Factor (LoRa)
- **TVS** - Transient Voltage Suppressor
- **WEEE** - Waste Electrical and Electronic Equipment

17 | Revision history

Revision	Date *(ISO 8601)*	Description
v1.0	2026-08-24	Initial ELPM-N54LW release

OBJEX