OBJEX

ELPM-S3LW

Extreme Low Power Module based on ESP32-S3FN8 and SX1262

v1.6 LW-B

DATASHEET

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Contents

1 | Overview

The ELPM-S3LW is an extreme-low power module based on the ESP32-S3FN8 and the SX1262, designed for the development of IoT devices and generic applications, especially battery-powered devices and energy harvesting applications. The module has a power unit designed to adapt to each specific use case, and together with the Deep Stop mode it is possible to minimize power consumption. It also integrates a crypto element (ATECC608C) that guarantees a high security standard, making the ELPM-S3LW an excellent choice for industrial applications and devices that require high energy efficiency.

1.1 | Features

Microcontroller

- Based on ESP32-S3FN8 (32-bit, 240 MHz)
- Memory size: 8 MB Flash
- GPIO: 34 available
- WiFi - IEEE 802.11 b/g/n-compliant
- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Wi-Fi and Bluetooth share the same antenna
- Cryptographic hardware acceleration
- External PSRAM can be installed
- Interfaces: I²C, I²S, SPI, UART, USB
- Native USB on pins 25/26 (external TVS suggested)
- RGB status LED (WS2812B): GPIO48
- Integrated I²C pull-up resistors
- U.FL connector (GHz): WiFi/Bluetooth, 50 Ω

Sub-GHz radio

- Based on SX1262
- Frequency bands: 862 MHz to 928 MHz
- Max output power: +22 dBm
- Transmission distance: up to 5 km (antenna and environment dependent)
- Air data rate: LoRa up to 62.5 kbps, (G)FSK up to 300 kbps
- TX current: 118 mA @ +22 dBm (typ)
- RX current: 4.6 mA (typ)
- U.FL connector (SUB_GHz), 50 Ω matched output
- Dedicated LDO2 3.3 V @ 300 mA
- Dedicated 3.3V supply pad
- Full compatibility with LoRa, LoRaWAN and generic sub-GHz protocols

Extreme-low power unit

- Dedicated LDO1 3.3 V @ 300 mA for the ESP32
- Wake and Master inputs: rising/falling edge detectors triggering the power latch
- 1-30 nA battery draw in Deep Stop (power latch only)
- Wake/Master inputs: 3.3 V max, high value resistance to GND (not floating)
- RTC RV-3028-C7: 45-100 nA when used as Deep Stop wake source
- Dedicated RTC power supply pad
- Battery level circuit (zero leakage current)

Security

- ATECC608C secure element
- Hardware secure key storage
- ECDSA sign/verify, ECDH (ECC P-256)
- SHA-256, AES-128
- User-configurable secure memory slots

1.2 | Deep Stop Mode (Extreme low power)

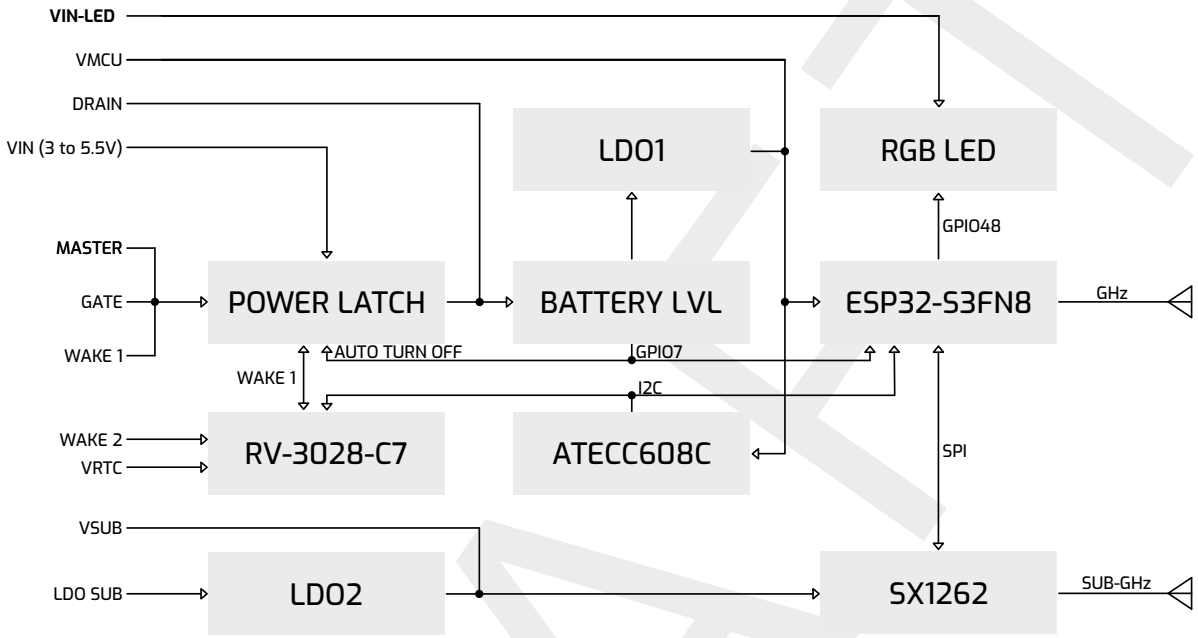
Deep Stop is an extreme-low power alternative to the ESP32-S3FN8 deep sleep. A power latch, triggered by the RTC or by the Wake/Master inputs, cuts the supply of the ESP32-S3FN8, the SX1262 and every load on the 3V3 path: while the system is off, the battery only feeds the power latch (1-30 nA) and, if used, the RTC (45-100 nA). The Gate pin can drive an external MOSFET to switch additional loads. Details in Section 6.

1.3 | Applications

The ELPM-S3LW fits a wide range of low-power applications, including the ones listed below. For some of them, ready-to-use KiCad reference designs (schematic and pre-configured project) are available in the OBJEX Labs GitHub repository: the linked applications can be clicked to download the corresponding project.

- Battery-powered nodes
- Smart meters
- Asset tracking
- Smart cities
- Street lights
- Supply chain
- Building automation
- Energy harvesting
- Smart agriculture
- Environmental sensors
- Predictive maintenance
- Cold chain monitoring
- Smart locks and access control
- Structural health monitoring
- Waste management
- Wireless alarm systems

2 | Block diagram



VMCU: Main power path for the ESP32-S3FN8.

VIN: Power path handled by the power latch, ideal for a battery.

Master: Power latch input: if the status changes (0 to 1 or 1 to 0), the power latch is triggered.

Gate: Power latch input: if low, the power latch is activated instantly.

Wake: Power latch input: if low, the power latch is triggered with a short startup delay.

Drain: Power latch: path between the control block and the input of the primary LDO.

AUTO TURN OFF: Input signal to trigger shutdown via the power latch.

VRTC: Power path reserved for the RV-3028-C7.

LDOSUB: LDO input reserved for the SX1262.

VSUB: Power path reserved for the SX1262.

VIN-LED: Power input for the internal RGB LED (located under the X of the logo). It is an input, not an output.

3 | Pin Definition

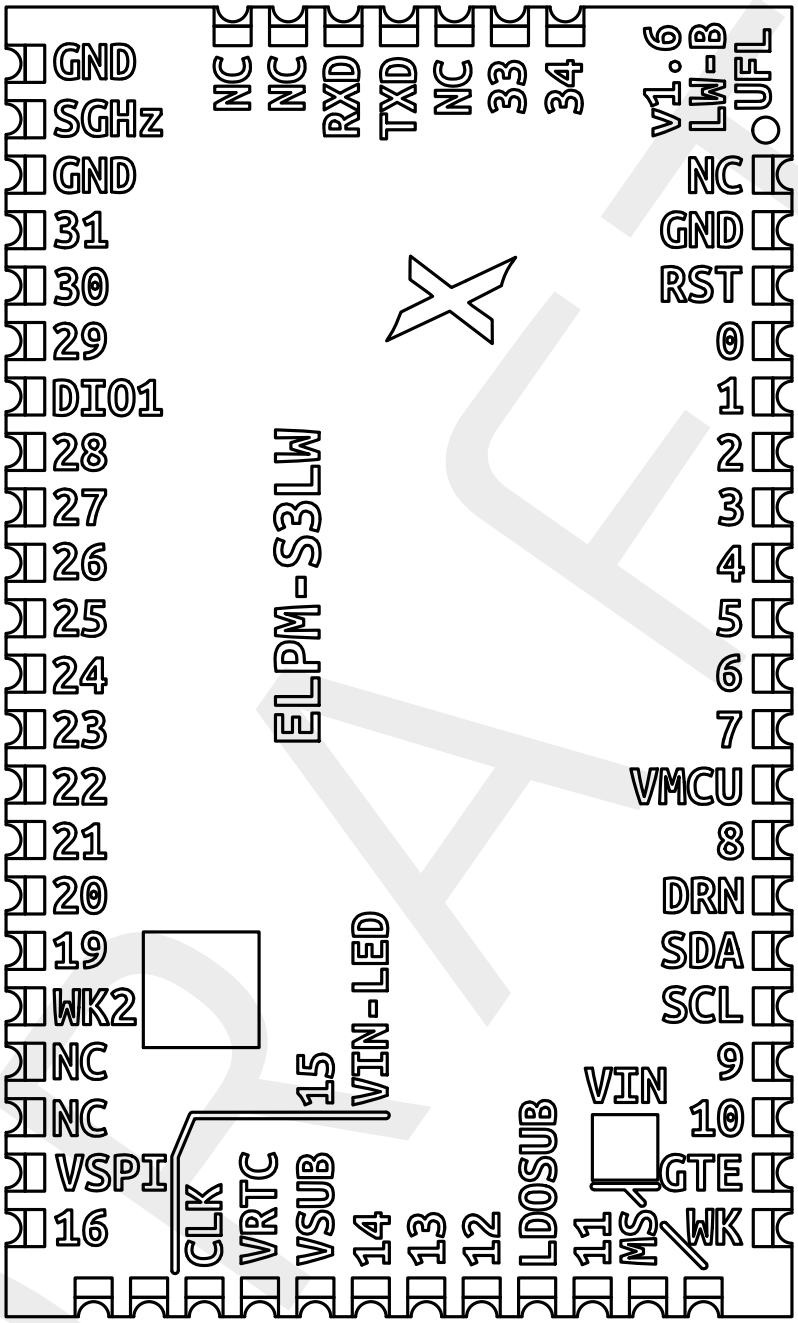


Figure 3.1: Pin names (bottom view)

3.1 | Pin Overview

The module has 62 castellated pins (1 to 60, plus A1 and A2) and 8 pads (ground only).

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
A1	GHz	RF	-	WiFi/Bluetooth antenna interface, impedance 50 Ω
A2	SUB_GHz	RF	-	Sub-GHz radio antenna interface, impedance 50 Ω

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
1	GND	P	-	Ground
2	RESET	I	3V3-RTC	ESP32-S3FN8 reset pin
3	0 (BOOT/GPIO)	I/O/T	3V3-RTC	RTC_GPIO0, GPIO0, **BOOT** strapping
4	1 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
5	2 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
6	3 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
7	4 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
8	5 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID
9	6 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0
10	7 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK
11	VMCU	P	-	ESP32-S3FN8 power supply (3V3)
12	8 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ
13	PLATCH_DRAIN	PL	-	Power latch drain
14	SDA/GPIO	I/O/T	3V3-RTC	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7, SUBSPICS1, **SDA**
15	SCL/GPIO	I/O/T	3V3-RTC	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, SUBSPIHD, **SCL**
16	10 (XTAL_P/GPIO)	I/O/T	3V3-RTC	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
17	9 (XTAL_N/GPIO)	I/O/T	3V3-RTC	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
18	PLATCH_GATE	PL	Vin	Power latch input
19	PLATCH_WAKE	PL	Vin	Power latch input
20	VIN	P	-	Power latch power supply
21	PLATCH_MASTER	PL	Vin	Power latch input
22	11 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6
23	LDOSUB	P	-	LDO2 input (sub-GHz radio)
24	12 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7
25	13 (D-/GPIO)	I/O/T	3V3-RTC	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, **USB_D-**
26	14 (D+/GPIO)	I/O/T	3V3-RTC	RTC_GPIO20, GPIO20, ADC2_CH9, CLK_OUT1, **USB_D+**
27	VSUB	P	-	Sub-GHz radio 3.3V power path
28	VRTC	P	-	RTC RV-3028-C7 power supply
29	RTC_CLK	O	VRTC	Clock output (RV-3028-C7)
30	VIN-LED	P	-	WS2812B power supply
31	15 (RGB/GPIO)	I/O/T	3V3-RTC	SPICLK_N_DIFF, GPIO48, SUBSPICLK_N_DIFF, **RGB LED**
32	16 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO21, GPIO21
33	VSPI	P	-	Output power supply: 1.8 V or VDD3P3_RTC

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
34	17 (NFC1/GPIO)[b]	-	-	NC on ELPM-S3LW
35	18 (NFC2/GPIO)[b]	-	-	NC on ELPM-S3LW
36	WK2 (RTC_EVI)	I	VRTC	RTC event input (RV-3028-C7 EVI)
37	19 (GPIO)	I/O/T	VDD	SPIHD, GPIO27
38	20 (GPIO)	I/O/T	VDD	SPIWP, GPIO28
39	21 (GPIO)	I/O/T	VDD	SPICS0, GPIO29
40	22 (GPIO)	I/O/T	VDD	SPICLK, GPIO30
41	23 (GPIO)	I/O/T	VDD	SPIQ, GPIO31
42	24 (GPIO)	I/O/T	VDD	SPID, GPIO32
43	25 (GPIO)	I/O/T	3V3-CPU/VDD	SPII04, GPIO33, FSPIHD, SUBSPIHD
44	26 (GPIO)	I/O/T	3V3-CPU/VDD	SPII05, GPIO34, FSPICS0, SUBSPICS0
45	27 (GPIO)	I/O/T	3V3-CPU/VDD	SPIDQS, GPIO37, FSPIQ, SUBSPIQ
46	28 (GPIO)	I/O/T	3V3-RTC	GPIO38, FSPIWP, SUBSPIWP
47	LORA_DIO1	I/O/T	VDD	**LORA_DIO1**, SPICLK_P_DIFF, GPIO47
48	29 (GPIO)	I/O/T	3V3-CPU	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
49	30 (GPIO)	I/O/T	3V3-CPU	**MTDO**, GPIO40, CLK_OUT2
50	31 (GPIO)	I/O/T	VDD	SPICS1, GPIO26
51	GND	P	-	Ground
52	GND	P	-	Ground
53	SWIO[b]	-	-	NC on ELPM-S3LW
54	SWCK[b]	-	-	NC on ELPM-S3LW
55	RXD	I/O/T	3V3-CPU	U0RXD, GPIO44, CLK_OUT2
56	TXD	I/O/T	3V3-CPU	U0TXD, GPIO43, CLK_OUT1
57	32 (NC)	-	-	NC
58	33 (GPIO)	I/O/T	3V3-CPU	**MTMS**, GPIO42
59	34 (GPIO)	I/O/T	3V3-CPU	**MTDI**, GPIO41, CLK_OUT1
60	GND	P	-	Ground
P1-P8	GND	P	-	Ground pads (bottom side)

[a] **P**: power supply; **RF**: radio frequency; **PL**: power latch; **I**: input; **O**: output; **T**: high impedance. Pin functions in **bold** font are the default pin functions.

[b] Reserved for other module variants of the ELPM family (not connected on the ELPM-S3LW). Module pin names are variant independent: for each pin the table reports the corresponding ESP32-S3FN8 signal of the ELPM-S3LW.

3.2 | Pin changes from revision v1.1

The castellated pin count and the mechanical dimensions are unchanged. Some pins have been renamed and some functions have been relocated. The table below lists the differences relevant when migrating a design from the previous revision; pins not listed are unchanged (renames of power pins aside).

No.	v1.1	v1.6	Migration note
11	3V3	VMCU	Renamed only
23	LDO-LORA	LDOSUB	Renamed only
26	GPIO26	GPIO20 (USB_D+)	GPIO26 is now on pin 50
27	3.3V-LORA	VSUB	Renamed only
28	VddRTC	VRTC	Renamed only
29	CLK	RTC_CLK	Renamed only
33	VDD	VSPI	Renamed only
34	GPIO20 (USB_D+)	NC	USB_D+ is now on pin 26
35	GPIO4 (LORA_RST)	NC	Sub-GHz radio SPI bus is now internal
36	GPIO5 (LORA_NSS)	WK2 (RTC_EVI)	Sub-GHz radio SPI bus is now internal
50	GPIO45 (LORA_SCK)	GPIO26	Sub-GHz radio SPI bus is now internal
53	GPIO36 (LORA_MOSI)	NC	Sub-GHz radio SPI bus is now internal
54	GPIO46 (LORA_BUSY)	NC	Sub-GHz radio SPI bus is now internal
57	GPIO35 (LORA_MISO)	NC	Sub-GHz radio SPI bus is now internal

3.3 | Strapping pins

At each startup or reset, the module requires some initial configuration parameters, such as the boot mode or the flash memory voltage. These parameters are passed via the strapping pins. After reset, the strapping pins operate as regular I/O pins. The parameters controlled by the strapping pins at module reset are as follows:

- Chip boot mode – GPIO0 and GPIO46
- VDD_SPI voltage – GPIO45
- ROM messages printing – GPIO46
- JTAG signal source – GPIO3

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset: these resistors determine the default bit values of the strapping pins. On the ELPM-S3LW only GPIO0 (pin 3, BOOT) and GPIO3 (pin 6) are exposed on castellated pins; GPIO45 and GPIO46 are managed internally.

For more details please read the official documentation of Espressif (ESP32-S3FN8).

3.4 | Pins used

Some GPIOs of the ESP32-S3FN8 are used to handle module features.

- SDA - GPIO8 (RTC, secure element)
- SCL - GPIO9 (RTC, secure element)
- Auto turn off - GPIO14
- Battery level – GPIO7
- Sub-GHz radio (SX1262) SPI bus - GPIO4 (RST), GPIO5 (NSS), GPIO35 (MISO), GPIO36 (MOSI), GPIO45 (SCK), GPIO46 (BUSY), internal only
- Sub-GHz radio DIO1 - GPIO47 (pin 47)

The I²C bus (GPIO8/GPIO9) is shared with the on-board peripherals but remains fully available for user applications; alternatively, a new I²C bus can be created from scratch on any free GPIOs.

Pins 25 (D-) and 26 (D+) expose the native USB interface of the ESP32-S3 (programming and USB CDC). An external TVS diode on the two USB lines is suggested for ESD protection.

4 | Electrical characteristics

4.1 | Absolute maximum ratings

Stresses beyond the values listed below may cause permanent damage to the module. These are stress ratings only; functional operation of the module at these or any other conditions beyond the recommended operating conditions is not implied. Values: TBD.

4.2 | Recommended operating conditions

To ensure the proper operation of the ELPM-S3LW, the following ranges must be observed.

Symbol	Parameter	Min	Max	Unit
VMCU	Power supply voltage (3V3 path)	3.0	3.6	V
VIN	Power latch or Battery input	3.0	5.5	V
LDOSUB	LDO2 input	3.0	5.5	V
VSUB	3.3V power path for the sub-GHz radio	3.0	3.5	V
VRTC	Power path for the RTC (RV-3028-C7)	3.0	3.3	V

4.3 | Maximum ESD ratings

Parameter	Min	Max	Unit
ESD immunity	2	12*	kV

* Maximum protection guaranteed only on the 3.3V path.

4.4 | Operating temperature range

Parameter	Min	Max	Unit
Operating temperature	-40	+85	°C

4.5 | GPIO DC characteristics

Digital I/O levels of the exposed GPIOs (ESP32-S3FN8 datasheet, VDD = 3.3 V):

Symbol	Parameter	Min	Max	Unit
VIH	High-level input voltage	0.75×VDD	VDD+0.3	V
VIL	Low-level input voltage	-0.3	0.25×VDD	V
VOH	High-level output voltage	0.8×VDD	-	V
VOL	Low-level output voltage	-	0.1×VDD	V

5 | RF characteristics

The module provides two independent antenna interfaces through U.FL connectors.

5.1 | Antenna interfaces

Connector	Radio	Impedance
GHz	WiFi/Bluetooth (ESP32-S3FN8)	50 Ω
SUB_GHz	Sub-GHz radio (SX1262)	50 Ω

5.2 | WiFi and Bluetooth (GHz)

- IEEE 802.11 b/g/n, 2.4 GHz
- Bluetooth 5 (LE), Bluetooth mesh

For detailed RF performance refer to the ESP32-S3 datasheet.

5.3 | Sub-GHz radio (SUB_GHz)

The sub-GHz radio supports LoRa, LoRaWAN and generic sub-GHz protocols. Typical values from the Semtech SX1262 datasheet:

Parameter	Condition	Value
Frequency bands	-	862 MHz to 928 MHz
TX output power	configurable	-9 dBm to +22 dBm
LoRa spreading factor	-	SF5 to SF12
LoRa bandwidth	-	7.8 kHz to 500 kHz
LoRa air data rate	-	up to 62.5 kbps
(G)FSK air data rate	-	0.6 kbps to 300 kbps
Sensitivity	LoRa, SF12, BW 10.4 kHz	-148 dBm
Sensitivity	LoRa, SF12, BW 125 kHz	-137 dBm
Sensitivity	LoRa, SF7, BW 125 kHz	-124 dBm
TX current	+22 dBm	118 mA (typ)
RX current	LoRa, BW 125 kHz	4.6 mA (typ)

For detailed RF performance refer to the SX1262 datasheet.

5.4 | Antenna requirements

Both interfaces require 50 Ω antennas connected through the U.FL receptacles. When selecting the antennas, the gain must be chosen so that the radiated power of the final product stays within the regulatory limits of the target region (for example ERP/EIRP limits of the EU 863-870 MHz band and of the 2.4 GHz band).

6 | Power management

The ELPM-S3LW integrates a smart power unit designed to reduce energy waste from the module and all components powered by it. Deep Stop mode is not intended to replace the deep sleep mode of the ESP32-S3, but is an additional solution that can be tailored during the development of a low-power device.

6.1 | Power consumption

Work mode	Description	Temp	Vin	Min	Typ	Unit
Deep Stop (RTC disabled)	Master, Gate or Wake input triggering the power latch. RTC not powered.	+20°C to +30°C	3.3V	<1	5	nA
Deep Stop with RTC	RTC powered. Multiple interrupt sources.	+20°C to +30°C	3.3V	40	80	nA
Deep sleep	Default deep sleep mode of the ESP32-S3.	+20°C to +30°C	3.3V	6	10	µA
Active	MCU running at 240 MHz, radios idle (measured).	+20°C to +30°C	3.3V	-	46	mA
Sub-GHz TX[a]	SX1262 transmitting @ +22 dBm.	+25°C	3.3V	-	118	mA
Sub-GHz RX[a]	SX1262 receiving (LoRa, BW 125 kHz).	+25°C	3.3V	-	4.6	mA

[a] Radio contribution only (SX1262 datasheet values): add the MCU current of the active work mode. For the WiFi and Bluetooth LE consumption refer to the ESP32-S3 datasheet.

6.2 | Auto turn off (power latch control)

When the system is powered through the power latch, the firmware controls the shutdown via the AUTO TURN OFF signal (GPIO14). The pin must be driven high and kept high for the whole phase that goes from the wake-up until the code intentionally decides to power the system off; driving it low triggers the shutdown through the power latch. This instruction must be given to the microcontroller as early as possible at startup: if AUTO TURN OFF is not asserted in time, the power latch may cut the supply and the system will turn off without ever starting.

6.3 | Startup time

The power latch is capable of booting the whole system in a few milliseconds, ensuring high reactivity. It is possible to reduce the startup time of the ESP32-S3 by tuning the boot options.

Interrupt mode	Description	Typ	Unit
Master P.Latch	Change of input status.	30	ms
RTC Wake	Scheduled wake-up.	80	ms
Gate	Gate input to GND.	20	ms
Wake	Wake input to GND.	500	ms

ESP32-S3FN8	Typ	Unit
Default startup time	105	ms

6.4 | Deep Stop performance

The following charts were measured with a Qoitech Otii Arc power analyzer. They show the wake-up times from Deep Stop and the consumption of the module when used in combination with the integrated RTC, with scheduled wake-up intervals that can be reconfigured via software, even at every power-on.

6.4.1 | Master/Wake mode

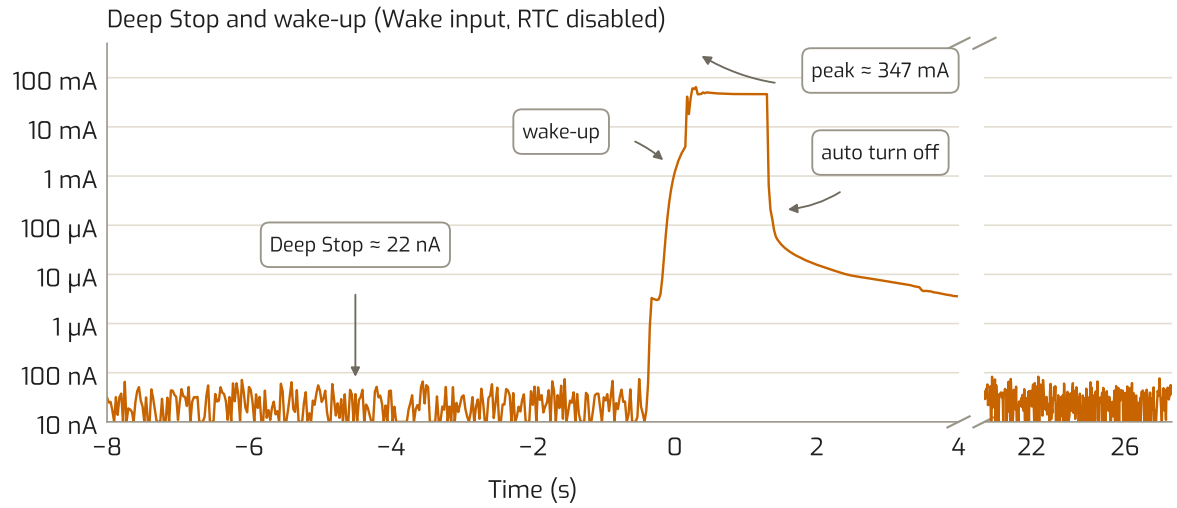


Figure 6.1: Deep Stop with the RTC disabled and wake-up from the Wake input (logarithmic current axis).

6.4.2 | System startup

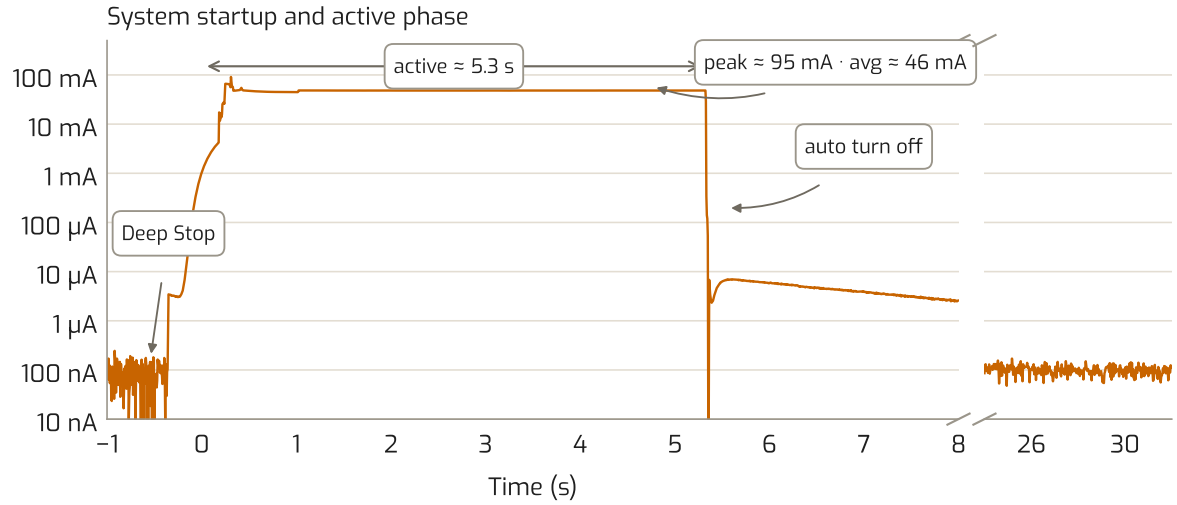


Figure 6.2: Detail of a single wake-up: startup, active phase and auto turn off (logarithmic current axis).

6.4.3 | RTC mode

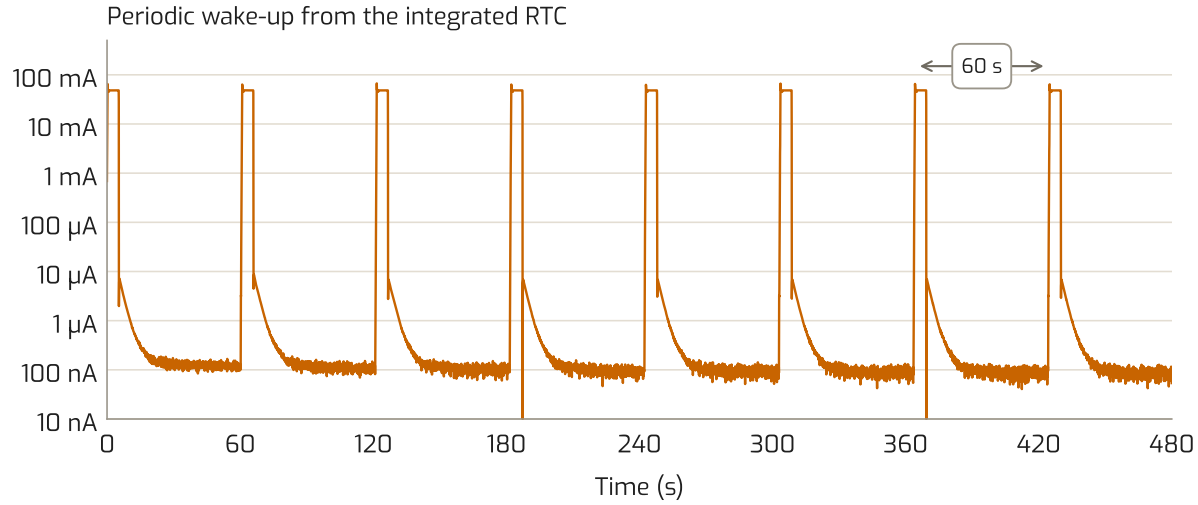


Figure 6.3: Wake-up every minute from the integrated RTC, nine consecutive cycles (logarithmic current axis).

7 | On-board peripherals

The module integrates the following peripherals: the RTC and the secure element, sharing the same I²C bus (SDA: GPIO8, SCL: GPIO9) with integrated pull-up resistors, the RGB status LED (WS2812B) and the battery level circuit.

7.1 | I²C address map

Device	Function	I²C address
RV-3028-C7	Real time clock	0x52
ATECC608C	Secure element	0x60

7.2 | RTC (RV-3028-C7)

Extreme low power external real time clock (45 nA to 100 nA), used by the Deep Stop mode for scheduled wake-up. It features a dedicated power supply pad (VRTC), a clock output (RTC_CLK pin) and an event input (WK2 pin, RV-3028-C7 EVI).

7.3 | Secure element (ATECC608C)

The ATECC608C is a secure element providing hardware-based secure key storage and cryptographic acceleration: ECDSA sign/verify and ECDH key agreement on the ECC P-256 curve, SHA-256, AES-128 and monotonic counters. The module mounts the standard I²C version of the device, shipped unprovisioned: key slots and configuration are fully available and their use is entirely at the discretion of the end user. Private keys can be generated directly inside the device and can never be read out: every cryptographic operation involving them is executed inside the silicon.

7.3.1 | Module authenticity

During provisioning the end user can give each module a unique, non-clonable cryptographic identity: a device certificate whose private key is generated and locked inside the secure element. The infrastructure can then verify the authenticity of the module at any time through a challenge-response mechanism: the module signs a random challenge with its private key and the verifier checks the signature against the device certificate chain. Periodic challenges allow the backend to continuously confirm that it is communicating with a genuine, untampered module.

7.3.2 | Example: MQTT with mutual TLS

An MQTT broker can be configured to require mutual TLS (mTLS): the module authenticates itself during the TLS handshake by signing with the private key stored in the ATECC608C, and access to specific topics can be restricted to authenticated clients only. Since the private key cannot be extracted or duplicated, the client identity cannot be forged.

7.3.3 | Sub-GHz security layer

The secure element also benefits the sub-GHz radio. For LoRaWAN the user can store the root keys in the device and use it to compute the AES-CMAC message integrity code. For proprietary sub-GHz protocols, transmitted messages can be signed (ECDSA) or authenticated (AES-CMAC), guaranteeing the authenticity and integrity of every frame and protecting the network from spoofing and tampering; monotonic counters can be used to prevent replay attacks.

7.3.4 | Regulatory context

The hardware root of trust provided by the secure element (unique device identity, protected key storage, verification of update authenticity) gives the final product a solid hardware foundation to meet the essential cybersecurity requirements of the EU Cyber Resilience Act (Regulation (EU) 2024/2847).

7.4 | RGB status LED (WS2812B)

Addressable RGB LED connected to GPIO48, located under the X of the logo and powered through the VIN-LED input.

7.5 | Battery level

Analog battery level circuit with zero leakage current, connected to GPIO7 (analog input).

8 | Software support

The module is based on the ESP32-S3 and is fully compatible with its standard development ecosystem: Arduino IDE, PlatformIO and ESP-IDF.

Ready-to-use firmware examples are available and maintained in the official OBJEX Labs GitHub repository:

github.com/OBJEX-Labs/OBJEX_ELPMs

Available examples:

- RGB status LED
- Power latch: Master/Wake inputs and auto turn off
- Power latch: RTC scheduled wake-up
- LoRaWAN node (RadioLib)
- LoRa point-to-point (ping-pong)

OBJEX also provides a dedicated support library that manages the on-board peripherals (RTC, RGB status LED, secure element, power latch) and other module features, and includes drivers for sensors commonly used with the module. The library does not constrain the development environment chosen by the user: it is a convenience layer to control the module in the most efficient way, and can be used alongside any of the supported ecosystems.

The GPIOs reserved for the module features are listed in Section 3.4.

8.1 | Programming interfaces

The module can be programmed through two interfaces:

- **UART0**: TXD (pin 56) and RXD (pin 55). To enter the serial download mode, hold BOOT (pin 3) low while releasing RESET (pin 2).
- **Native USB**: D- (pin 25) and D+ (pin 26), exposing the built-in USB Serial/JTAG controller of the ESP32-S3 (programming, USB CDC console and JTAG debug). An external TVS diode on the two USB lines is suggested.

Both interfaces are supported by the standard Espressif flashing tools (esptool, Arduino IDE, PlatformIO, ESP-IDF).

9 | Typical applications

The following reference schematics show typical supply configurations of the ELPM-S3LW.

9.1 | Direct constant supply

Constant power supply on the 3V3 path, power latch excluded.

Schematic: TBD.

9.2 | Battery supply with power latch, sensor as wake source

Battery powered through the power latch: an external sensor triggers the Wake input and turns the system on only when an event occurs.

Schematic: TBD.

9.3 | Battery supply with power latch and periodic RTC wake-up

Battery powered through the power latch: a sensor (for example a temperature sensor) is switched off together with the system and read at each periodic wake-up scheduled by the RTC.

Schematic: TBD.

10 | Design guidelines

10.1 | Module placement and layout

- Follow the recommended PCB footprint (Section 11.4).
- Do not route signal traces or place vias on the top layer of the host board under the module body: keep the area limited to the footprint pads and to a solid ground pour.
- Connect the ground pads on the bottom side of the module to a solid ground plane.
- Leave enough clearance around the castellated edges for soldering inspection and rework.
- Keep the area around the two U.FL receptacles clear, so that the coaxial plugs can be mated and the cables routed without stress.

10.2 | Antenna connections

Both RF interfaces use the same standard U.FL coaxial receptacle (50 Ω) soldered on the module. To connect the antennas, use 50 Ω cable assemblies terminated with a standard U.FL mating plug (Hirose U.FL-LP series or compatible). Note that this connector family is rated for a limited number of mating cycles (typically 30): use the dedicated extraction tool and avoid unnecessary connect/disconnect cycles.

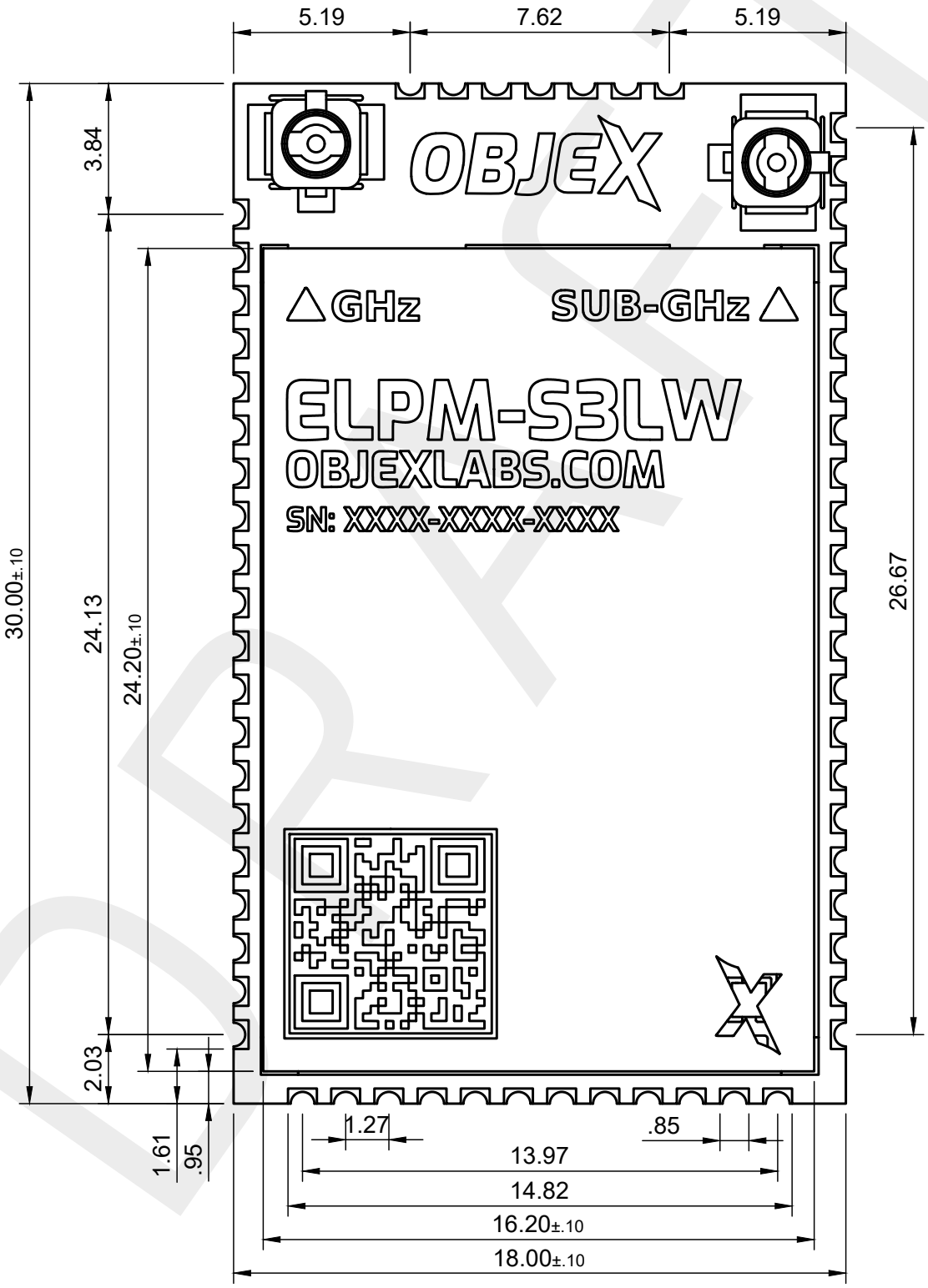
10.3 | External circuitry

- USB: an external TVS diode on the D+/D- lines (pins 25/26) is suggested for ESD protection.
- Wake/Master inputs: maximum 3.3 V, driven through a high value resistance to GND (never floating); keep the traces short to avoid spurious wake-up events.
- Power input: place a local bulk capacitor close to the VIN pin when the supply cable is long or the battery has a high internal resistance.

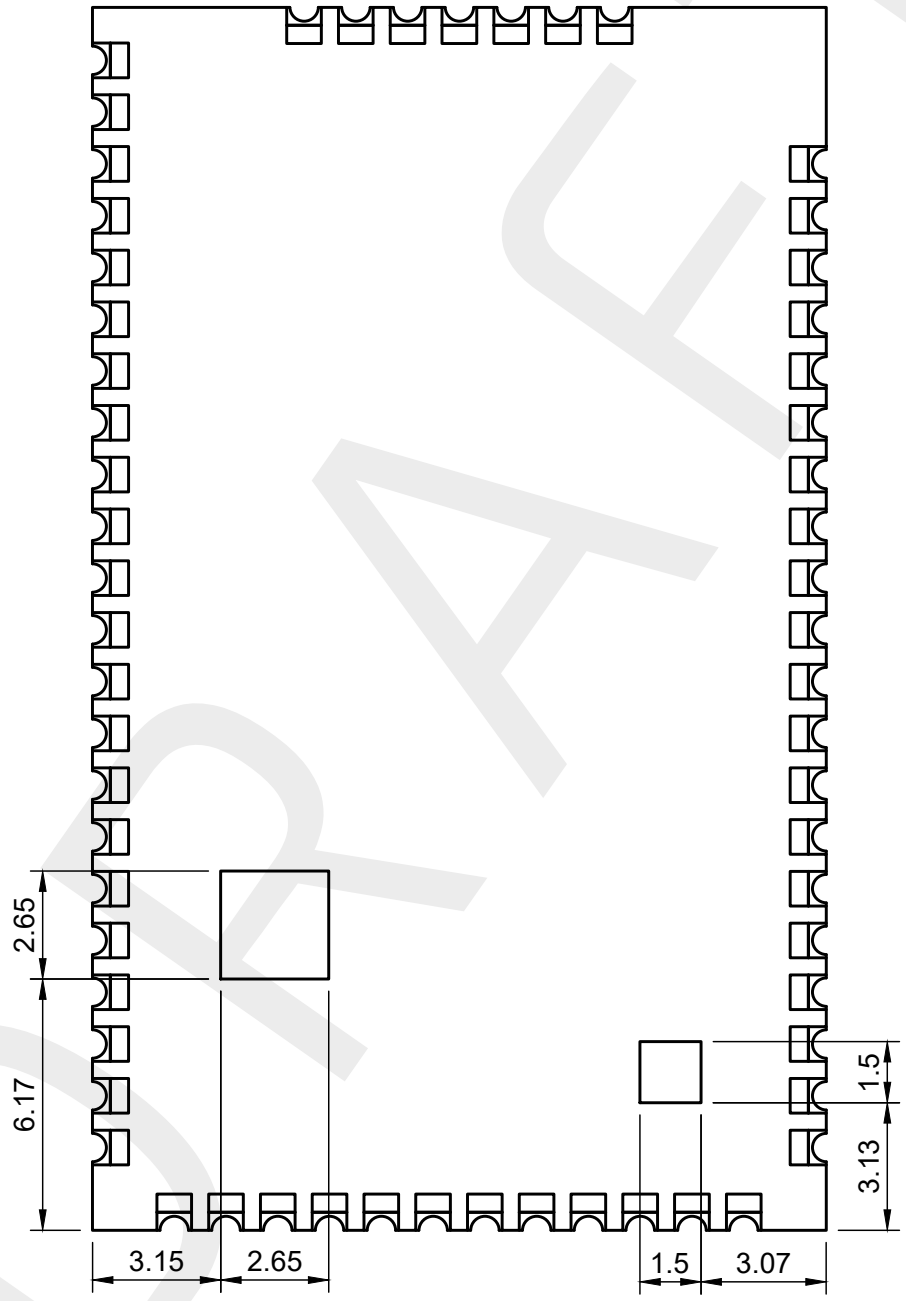
11 | Physical Dimensions

Dimensions in millimeters.

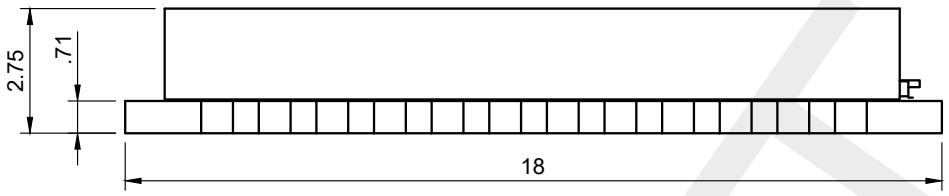
11.1 | Top view



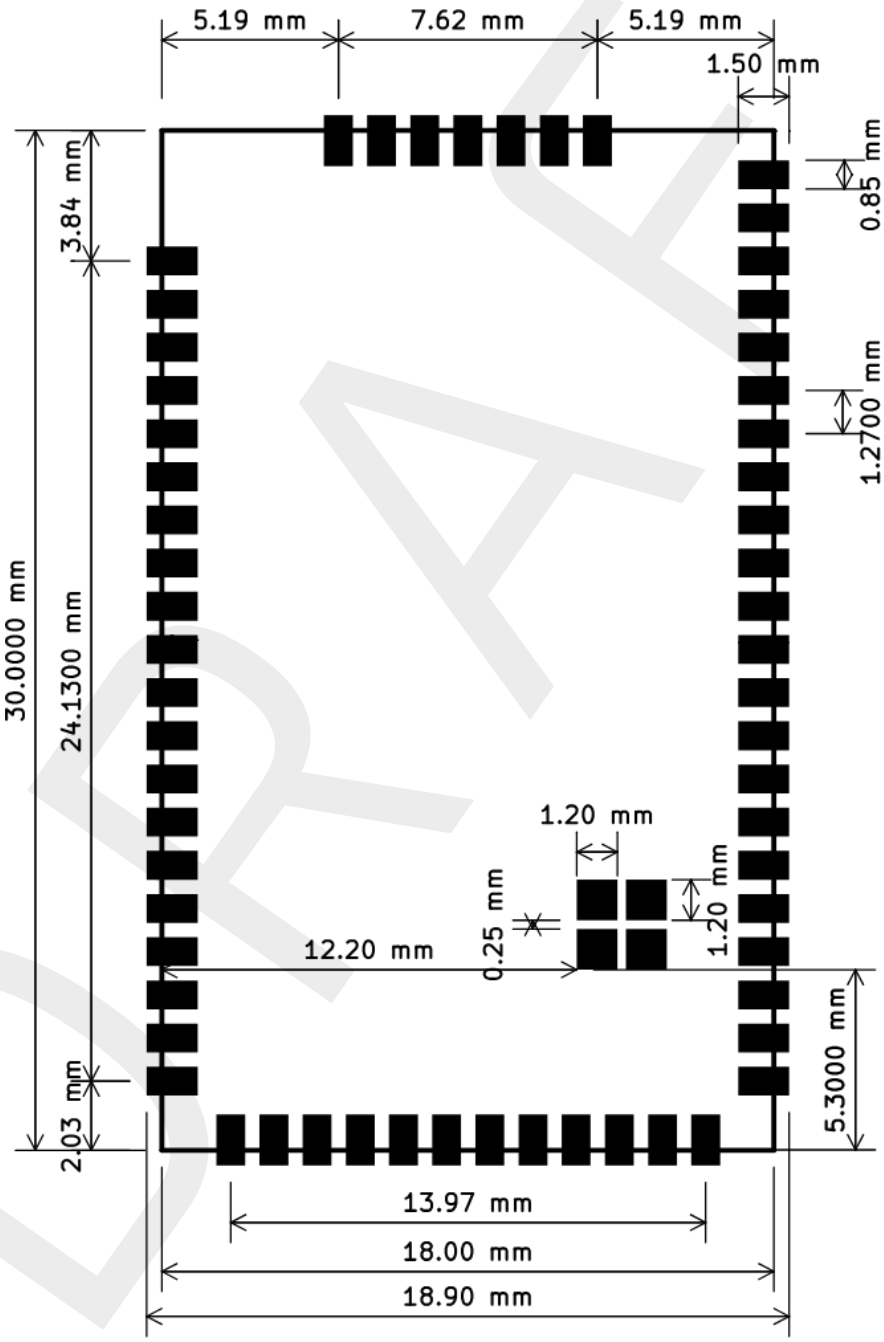
11.2 | Bottom view



11.3 | Side view



11.4 | Recommended PCB footprint



12 | Soldering and handling

12.1 | Reflow soldering

The module is assembled with a lead-free SAC-type solder alloy (melting point approximately 217 °C). To prevent the internal solder joints of the module from re-melting during board assembly, the use of a low-temperature lead-free solder paste (SnBi or SnBiAg alloys, melting point approximately 138 °C) is recommended, keeping the peak temperature at or below 210 °C.

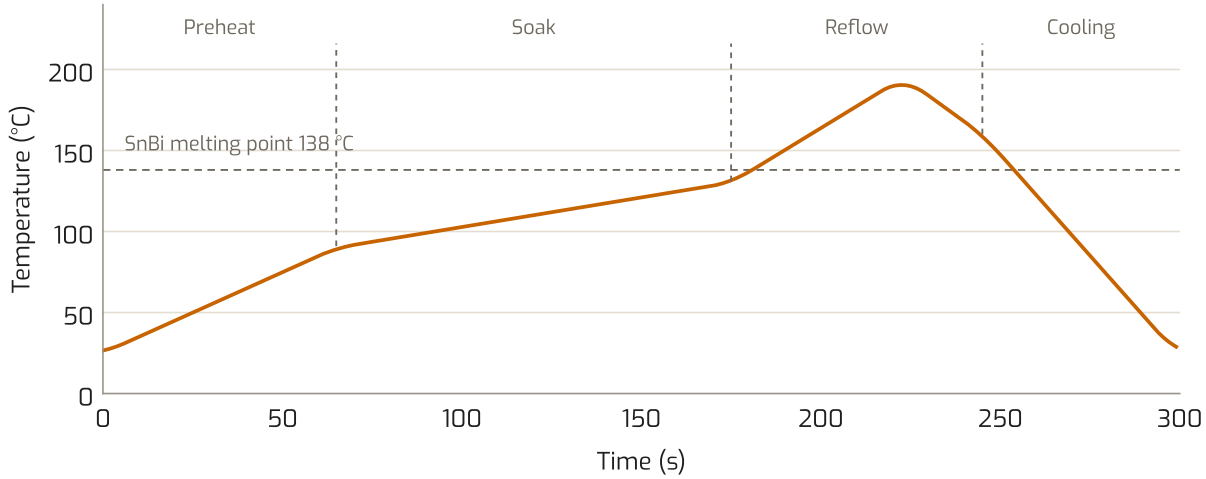


Figure 12.1: Recommended low-temperature reflow profile.

Profile parameter	Recommended value
Ramp-up rate	≤ 2 °C/s
Preheat/soak	90 s to 120 s, 90 °C to 130 °C
Peak temperature	180 °C to 210 °C
Time above melting point (138 °C)	45 s to 75 s
Ramp-down rate	≤ 3 °C/s
Maximum reflow cycles	2

If the assembly process requires a standard lead-free profile (IPC/JEDEC J-STD-020), the peak temperature must never exceed 245 °C and the module must not be exposed to more than two reflow cycles. In this case the internal joints of the module can re-melt during the process: avoid any mechanical shock or vibration until the assembly has cooled down.

12.2 | Moisture sensitivity

Moisture sensitivity level (MSL): TBD.

12.3 | Storage conditions

Recommended storage conditions: TBD.

12.4 | ESD handling precautions

The module is an electrostatic discharge sensitive device. Handle it only at ESD-protected workstations (grounded wrist strap, dissipative surfaces) in accordance with IEC 61340-5-1 or ANSI/ESD S20.20, and keep it in its original protective packaging until assembly.

13 | Ordering information

Preliminary: order codes and packaging details will be finalized before mass production.

Order code	Description	Packaging
ELPM-S3LW	ESP32-S3FN8 + SX1262 sub-GHz radio, ATECC608C	Bulk (ESD bag)

13.1 | Product marking

Each module is marked on the top overlay with the product name, the manufacturer website and a unique serial number (SN: XXXX-XXXX-XXXX). The QR code encodes the serial number, allowing fast identification and unit-level traceability.

14 | Certifications

Certification activities are in progress: internal verification is being completed before laboratory testing. The table below will be updated as the activities progress.

Certification	Region	Status
CE (RED)	Europe	In progress

14.1 | Material compliance (RoHS, REACH)

The module is designed and manufactured to comply with Directive 2011/65/EU (RoHS 2) as amended by Directive (EU) 2015/863, and with Regulation (EC) 1907/2006 (REACH). Compliance declarations will be made available together with the product certifications.

14.2 | WEEE (RAEE)

In accordance with Directive 2012/19/EU on waste electrical and electronic equipment (WEEE, implemented in Italy as RAEE), this product must not be disposed of with unsorted municipal waste at the end of its life. The crossed-out wheeled bin symbol indicates that the product is subject to separate collection: return it to an authorized collection point or to the distributor for proper treatment, recovery and recycling.

15 | Related documentation

- ESP32-S3 Series - Microcontroller
- SX1262 - Sub-GHz radio IC
- RV-3028-C7 - Extreme low power ext. RTC
- ATECC608C - Secure element
- WS2812B - RGB status LED

16 | Acronyms

- **ADC** - Analog to Digital Converter
- **BLE** - Bluetooth Low Energy
- **CDC** - Communications Device Class (USB)
- **EIRP** - Effective Isotropic Radiated Power
- **ERP** - Effective Radiated Power
- **ESD** - Electrostatic Discharge
- **(G)FSK** - (Gaussian) Frequency Shift Keying
- **GPIO** - General Purpose Input/Output
- **LDO** - Low Dropout regulator
- **MSL** - Moisture Sensitivity Level
- **mTLS** - mutual Transport Layer Security
- **NC** - Not Connected
- **RTC** - Real Time Clock
- **SF** - Spreading Factor (LoRa)
- **TVS** - Transient Voltage Suppressor
- **WEEE** - Waste Electrical and Electronic Equipment

17 | Revision history

Revision	Date *(mm/dd/yyyy)*	Description
v1.6	08/12/2026	Hardware revision: ATECC608C secure element added, U.FL nomenclature updated (GHz, SUB_GHz), pin naming and placement updates. Document restructured and fully revised
v1.1	07/06/2024	Add example Firmware section
v1.1	04/18/2024	Power consumption graphs, general bugfix (document still being finalized - draft)
v1.0	03/05/2024	Updated the value frequency bands 862MHz to 928MHz
v1.0	02/26/2024	Preliminary version for partners

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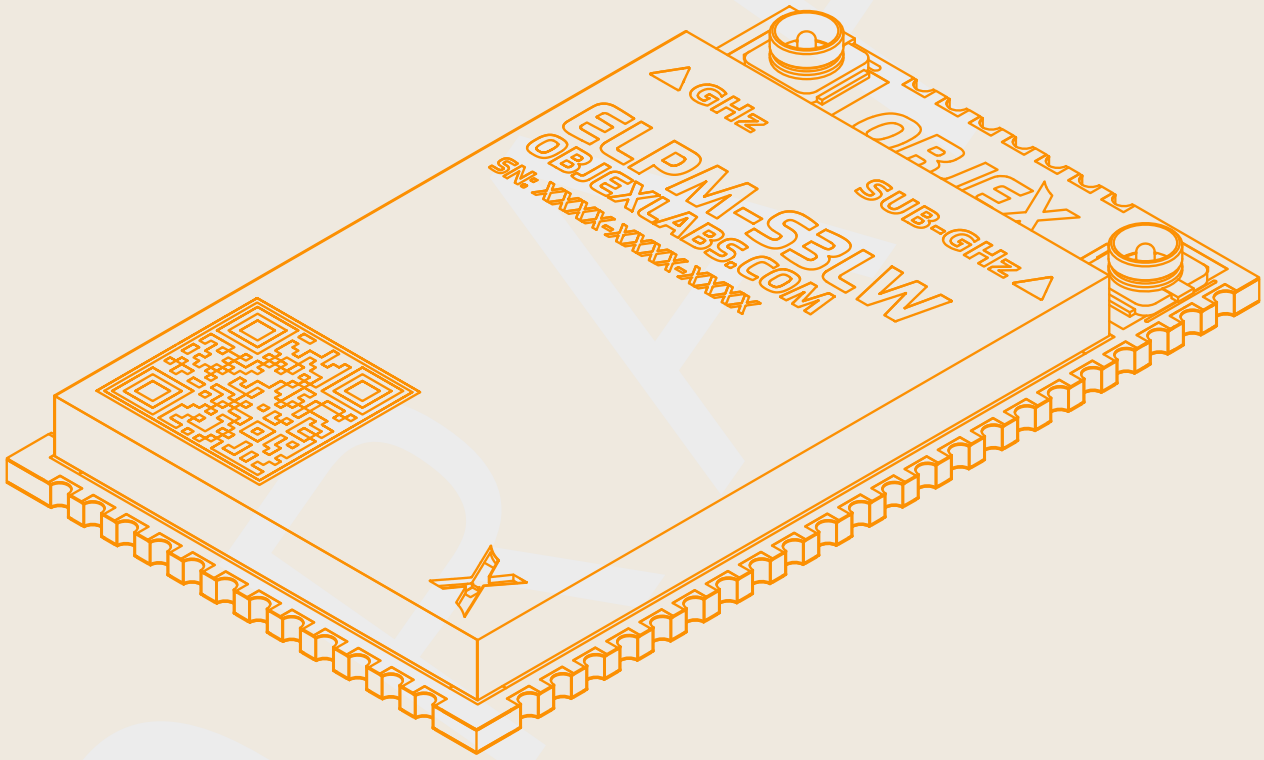

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