OBJEX

ELPM-S3LW

Extreme Low Power Module based on ESP32-S3FN8 and SX1262

v1.6 LW-B

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DATASHEET

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1 | Overview

The ELPM-S3LW is an extreme-low power module based on the ESP32-S3FN8 and the SX1262, designed for the development of IoT devices and generic applications, especially battery-powered devices and energy harvesting applications. The module has a power unit designed to adapt to each specific use case, and together with the Deep Stop mode it is possible to minimize power consumption. It also integrates a crypto element (ATECC608C) that guarantees a high security standard, making the ELPM-S3LW an excellent choice for industrial applications and devices that require high energy efficiency.

1.1 | Features

Microcontroller

- Based on ESP32-S3FN8 (32-bit, 240 MHz)
- Memory size: 8 MB Flash
- GPIO: 34 available
- WiFi - IEEE 802.11 b/g/n-compliant
- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Wi-Fi and Bluetooth share the same antenna
- Cryptographic hardware acceleration
- External PSRAM can be installed
- Interfaces: I²C, I²S, SPI, UART, USB
- Native USB on pins 25/26 (external TVS suggested)
- RGB status LED (WS2812B): GPIO48
- Integrated 10 kΩ I²C pull-up resistors to VMCU
- U.FL connector (GHz): WiFi/Bluetooth, 50 Ω

Sub-GHz radio

- Based on SX1262
- Frequency bands: 862 MHz to 928 MHz
- Max output power: +22 dBm
- Transmission distance: up to 5 km (antenna and environment dependent)
- Air data rate: LoRa up to 62.5 kbps, (G)FSK up to 300 kbps
- TX current: 118 mA @ +22 dBm (typ)
- RX current: 4.6 mA (typ)
- U.FL connector (SUB_GHz), 50 Ω matched output
- Dedicated LDO2 3.3 V @ 300 mA
- Dedicated 3.3V supply pad
- Full compatibility with LoRa, LoRaWAN and generic sub-GHz protocols

Extreme-low power unit

- On-board LDO1: 3.3 V, 300 mA total rail capacity
- VMCU rail supplies the ESP32-S3FN8 and ATECC608C
- WAKE and MASTER inputs: rising/falling edge detectors triggering the power latch
- 1–30 nA battery draw in Deep Stop (power latch only)
- WAKE/MASTER inputs: 3.3 V max, high value resistance to GND (not floating)
- RTC RV-3028-C7: 45–100 nA when used as Deep Stop wake source
- Dedicated RTC power supply pad
- Battery-level input on GPIO7 through a 2 × 100 kΩ resistive divider

Security

- ATECC608C secure element
- Hardware secure key storage
- ECDSA sign/verify, ECDH (ECC P-256)
- SHA-256, AES-128
- User-configurable secure memory slots

1.2 | Deep Stop Mode (Extreme low power)

Deep Stop is an extreme-low power alternative to the ESP32-S3FN8 deep sleep. A power latch, triggered by the RTC or by the WAKE/MASTER inputs, cuts the supply of the ESP32-S3FN8, the SX1262 and every load on the 3V3 path: while the system is off, the battery only feeds the power latch (1–30 nA) and, if used, the RTC (45–100 nA). The GATE pin can drive an external MOSFET to switch additional loads. Details in Section 6.

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1.3 | Applications

The ELPM-S3LW fits a wide range of low-power applications, including the ones listed below. For some of them, ready-to-use KiCad reference designs (schematic and pre-configured project) are available in the OBJEX Labs GitHub repository: the linked applications can be clicked to download the corresponding project.

- Battery-powered nodes
- Smart meters
- Asset tracking
- Smart cities
- Street lights
- Supply chain
- Building automation
- Energy harvesting
- Smart agriculture
- Environmental sensors
- Predictive maintenance
- Cold chain monitoring
- Smart locks and access control
- Structural health monitoring
- Waste management
- Wireless alarm systems

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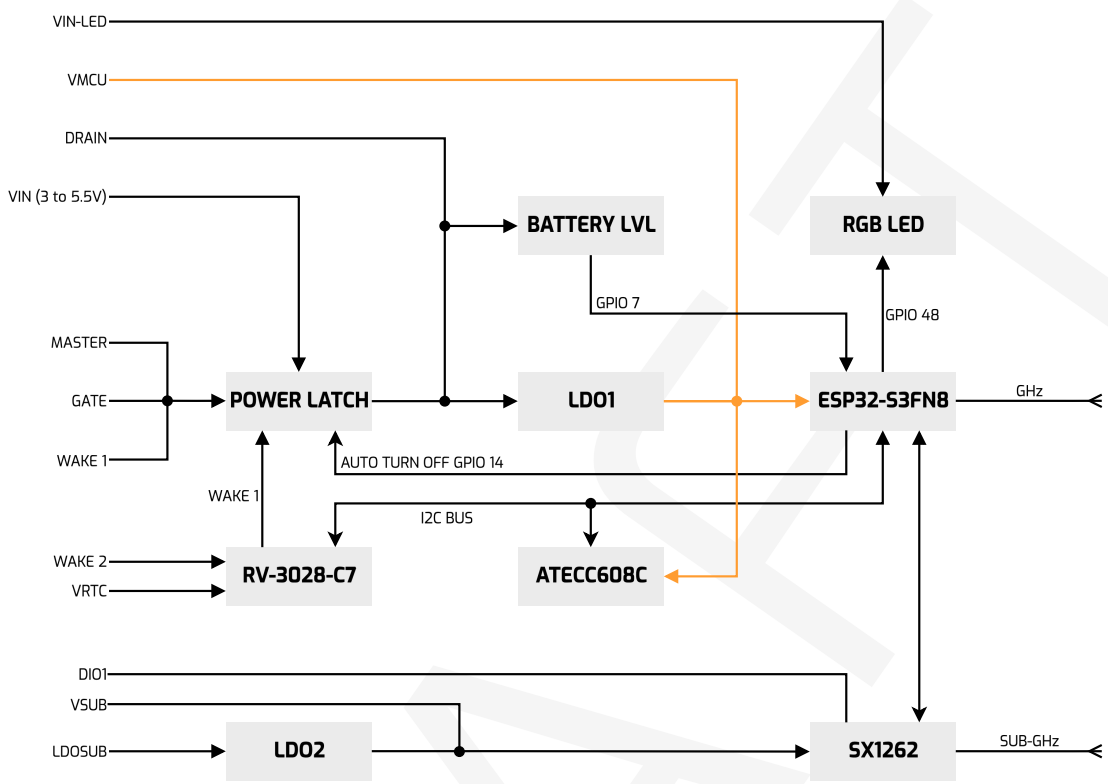
2 | Block diagram



VMCU: Shared ESP32-S3FN8 and ATECC608C rail; direct 3.3 V input or regulated output, depending on the supply configuration.

VIN: Power path handled by the power latch, ideal for a battery.

MASTER: Power latch input: if the status changes (0 to 1 or 1 to 0), the power latch is triggered.

GATE: Power latch input: if low, the power latch is activated instantly.

WAKE: Power latch input: if low, the power latch is triggered with a short startup delay.

DRAIN: Unregulated switched copy of VIN; it may supply LDOSUB when the Sub-GHz radio must follow the power-latch state. Its voltage is nominally equal to VIN apart from a small internal path drop, and the pin becomes high-impedance when the latch is off.

AUTO TURN OFF: In VIN power-latch mode, this firmware-controlled signal holds the latch on when high and requests shutdown when low. While held high, further MASTER, WAKE and GATE events are ignored. It does not control the supply in direct VMCU mode.

VRTC: External supply for the RV-3028-C7. The module has no internal RTC backup battery; removing VRTC stops timekeeping and the stored date and time are lost.

WAKE 1: Direct external input to the power-latch wake path.

WAKE2: External event input of the RV-3028-C7. When VRTC is supplied, an event on this pin or an internally programmed RTC timer/alarm asserts RTC INT, which reaches the same power-latch wake path.

LDOSUB: Input of the Sub-GHz supply path; leave VSUB floating when using the on-board LDO.

VSUB: SX1262 supply rail; for direct regulated supply, connect VSUB and LDOSUB together to the external source. VMCU may use the same source or a separate compatible supply.

VIN-LED: 3.5-5.5 V power input for the internal RGB LED (located under the X of the logo). It is an input, not an output.

3 | Pin Definition

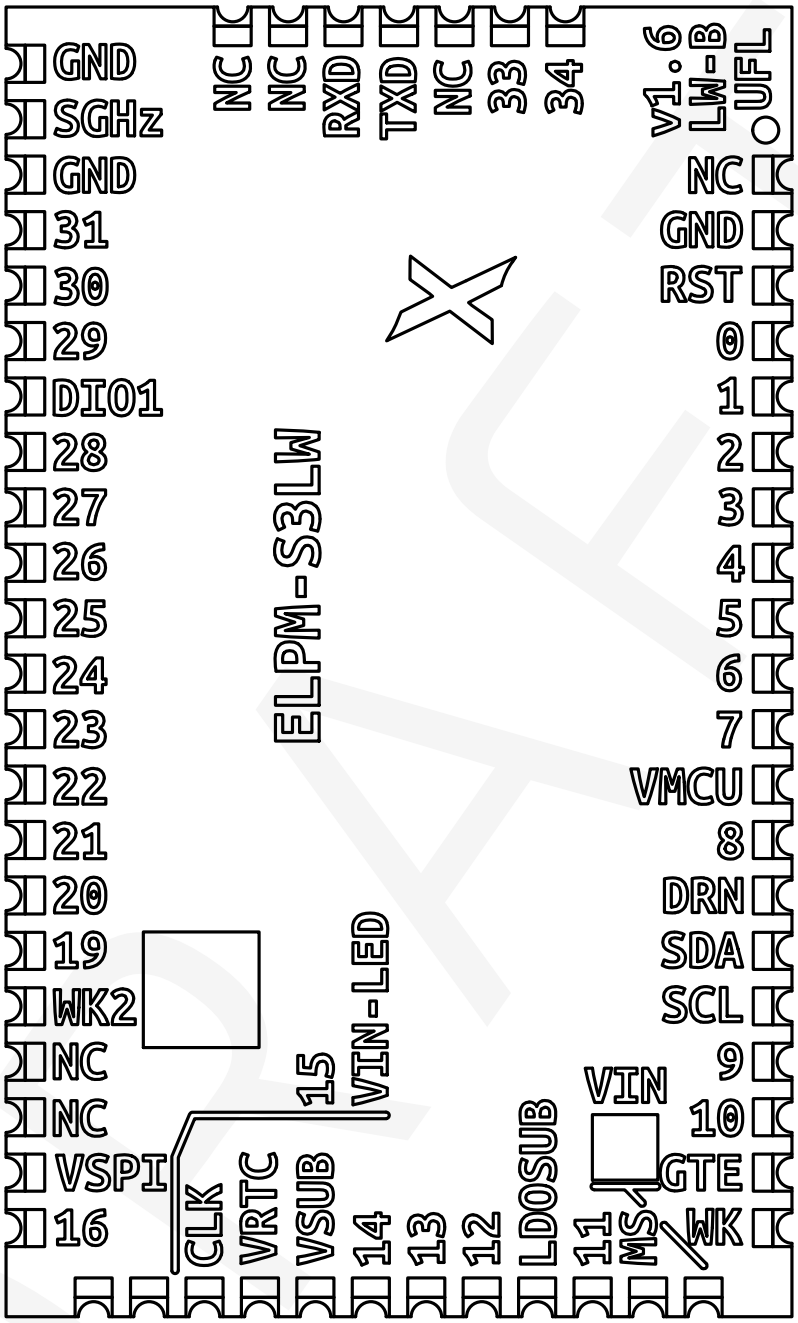


Figure 3.1: Pin names (bottom view)

3.1 | Pin Overview

The module has 62 castellated pins (1 to 60, plus A1 and A2) and two auxiliary contacts on the bottom side, one connected to VIN and one connected to GND.

ELPM-S3LW and ELPM-N54LW use the same mechanical footprint and castellated-pin numbering. The common carrier-board interface includes GND, RESET, VMCU, VIN, PLATCH_DRAIN, PLATCH_GATE, PLATCH_WAKE, PLATCH_MASTER, SDA, SCL, VSUB, VRTC, RTC_CLK, WAKE2, LORA_DIO1 and SUB_GHz; pins 55 and 56 also retain RXD and TXD roles. A carrier board restricted to these common interfaces can accommodate either module when the supply, current and logic-level requirements of the installed variant are satisfied. MCU-specific GPIO assignments, A1 RF connectivity, NC pins,

optional power pins and firmware are variant dependent and shall be reviewed before substitution.

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
A1	GHz	RF	-	WiFi/Bluetooth antenna interface, impedance 50 Ω
A2	SUB_GHz	RF	-	Sub-GHz radio antenna interface, impedance 50 Ω
1	GND	P	-	Ground
2	RESET	I	3V3-RTC	ESP32-S3FN8 reset pin
3	0 (BOOT/GPIO)	I/O/T	3V3-RTC	RTC_GPIO0, GPIO0, **BOOT** strapping
4	1 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
5	2 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
6	3 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
7	4 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
8	5 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID
9	6 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0
10	7 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK
11	VMCU	P	-	3.3 V supply input in direct mode; on-board LDO output in VIN power-latch mode
12	8 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ
13	PLATCH_DRAIN	PL	VIN	Unregulated switched VIN path; high-impedance when off; 1 A absolute maximum
14	SDA/GPIO	I/O/T	3V3-RTC	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7, SUBSPICS1, **SDA**
15	SCL/GPIO	I/O/T	3V3-RTC	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, SUBSPIHD, **SCL**
16	10 (XTAL_P/GPIO)	I/O/T	3V3-RTC	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
17	9 (XTAL_N/GPIO)	I/O/T	3V3-RTC	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
18	PLATCH_GATE	PL	VIN	Power latch input
19	PLATCH_WAKE	PL	VIN	Power latch input
20	VIN	P	-	Power latch and on-board LDO input, 5.5 V maximum
21	PLATCH_MASTER	PL	VIN	Power latch input
22	11 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6
23	LDOSUB	P	-	Sub-GHz LDO supply input; not a power output
24	12 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7
25	13 (D-/GPIO)	I/O/T	3V3-RTC	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, **USB_D-**

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
26	14 (D+/GPIO)	I/O/T	3V3-RTC	RTC_GPIO20, GPIO20, ADC2_CH9, CLK_OUT1, **USB_D+**
27	VSUB	P	-	Direct Sub-GHz radio supply input; not a power output
28	VRTC	P	-	RTC supply input; not a power output
29	RTC_CLK	O	VRTC	Clock output (RV-3028-C7)
30	VIN-LED	P	-	WS2812B-1010 supply input, 3.5-5.5 V; not a power output
31	15 (RGB/GPIO)	I/O/T	3V3-RTC	SPICLK_N_DIFF, GPIO48, SUBSPICLK_N_DIFF, **RGB LED DIN**; internal LED DOUT not connected
32	16 (GPIO)	I/O/T	3V3-RTC	RTC_GPIO21, GPIO21
33	VSPI	P	-	Output power supply: 1.8 V or VDD3P3_RTC
34	17 (NFC1/GPIO)[b]	-	-	NC on ELPM-S3LW
35	18 (NFC2/GPIO)[b]	-	-	NC on ELPM-S3LW
36	WAKE2 (RTC_EVI)	I	VRTC	Active-high RTC event input; internal 10 kΩ pull-down; requires VRTC
37	19 (GPIO)	I/O/T	VDD	SPIHD, GPIO27
38	20 (GPIO)	I/O/T	VDD	SPIWP, GPIO28
39	21 (GPIO)	I/O/T	VDD	SPICS0, GPIO29
40	22 (GPIO)	I/O/T	VDD	SPICLK, GPIO30
41	23 (GPIO)	I/O/T	VDD	SPIQ, GPIO31
42	24 (GPIO)	I/O/T	VDD	SPID, GPIO32
43	25 (GPIO)	I/O/T	3V3-CPU/VDD	SPII04, GPIO33, FSPIHD, SUBSPIHD
44	26 (GPIO)	I/O/T	3V3-CPU/VDD	SPII05, GPIO34, FSPICS0, SUBSPICS0
45	27 (GPIO)	I/O/T	3V3-CPU/VDD	SPIDQS, GPIO37, FSPIQ, SUBSPIQ
46	28 (GPIO)	I/O/T	3V3-RTC	GPIO38, FSPIWP, SUBSPIWP
47	LORA_DIO1	I/O/T	VDD	**LORA_DIO1**, SPICLK_P_DIFF, GPIO47
48	29 (GPIO)	I/O/T	3V3-CPU	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
49	30 (GPIO)	I/O/T	3V3-CPU	**MTDO**, GPIO40, CLK_OUT2
50	31 (GPIO)	I/O/T	VDD	SPICS1, GPIO26
51	GND	P	-	Ground
52	GND	P	-	Ground
53	SWIO[b]	-	-	NC on ELPM-S3LW
54	SWCK[b]	-	-	NC on ELPM-S3LW
55	RXD	I/O/T	3V3-CPU	U0RXD, GPIO44, CLK_OUT2
56	TXD	I/O/T	3V3-CPU	U0TXD, GPIO43, CLK_OUT1
57	32 (NC)	-	-	NC
58	33 (GPIO)	I/O/T	3V3-CPU	**MTMS**, GPIO42
59	34 (GPIO)	I/O/T	3V3-CPU	**MTDI**, GPIO41, CLK_OUT1
60	GND	P	-	Ground
AUX-VIN	VIN	P	-	Auxiliary VIN contact (bottom side)

No.	Name	Type[a]	Power Domain	Function (ESP32-S3FN8)
AUX-GND	GND	P	-	Auxiliary ground contact (bottom side)

[a] **P**: power supply; **RF**: radio frequency; **PL**: power latch; **I**: input; **O**: output; **T**: high impedance. Pin functions in **bold** font are the default pin functions.

[b] Reserved for other module variants of the ELPM family (not connected on the ELPM-S3LW). Module pin names are variant independent: for each pin the table reports the corresponding ESP32-S3FN8 signal of the ELPM-S3LW.

The auxiliary bottom contacts are intended for soldering wires directly to the module in point-to-point prototypes or assemblies without a complete host PCB. AUX-VIN is electrically the same supply input as VIN and is subject to the same ratings and power-latch behaviour. AUX-GND is connected to module GND. These contacts are intentionally omitted from the recommended host-PCB footprint; conventional PCB assemblies shall use the castellated VIN and GND pins.

3.2 | Pin changes from revision v1.1

The castellated pin count and the mechanical dimensions are unchanged. Some pins have been renamed and some functions have been relocated. The table below lists the differences relevant when migrating a design from the previous revision; pins not listed are unchanged (renames of power pins aside).

No.	v1.1	v1.6	Migration note
11	3V3	VMCU	Renamed only
23	LDO-LORA	LDOSUB	Renamed only
26	GPIO26	GPIO20 (USB_D+)	GPIO26 is now on pin 50
27	3.3V-LORA	VSUB	Renamed only
28	VddRTC	VRTC	Renamed only
29	CLK	RTC_CLK	Renamed only
33	VDD	VSPI	Renamed only
34	GPIO20 (USB_D+)	NC	USB_D+ is now on pin 26
35	GPIO4 (LORA_RST)	NC	Sub-GHz radio SPI bus is now internal
36	GPIO5 (LORA_NSS)	WAKE2 (RTC_EVI)	Sub-GHz radio SPI bus is now internal
50	GPIO45 (LORA_SCK)	GPIO26	Sub-GHz radio SPI bus is now internal
53	GPIO36 (LORA_MOSI)	NC	Sub-GHz radio SPI bus is now internal
54	GPIO46 (LORA_BUSY)	NC	Sub-GHz radio SPI bus is now internal
57	GPIO35 (LORA_MISO)	NC	Sub-GHz radio SPI bus is now internal

3.3 | Strapping pins

At each startup or reset, the module requires some initial configuration parameters, such as the boot mode or the flash memory voltage. These parameters are passed via the strapping pins. After reset, the strapping pins operate as regular I/O pins. The parameters controlled by the strapping pins at module reset are as follows:

- Chip boot mode – GPIO0 and GPIO46
- VDD_SPI voltage – GPIO45
- ROM messages printing – GPIO46
- JTAG signal source – GPIO3

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset: these resistors determine the default bit values of the strapping pins. On the ELPM-S3LW only GPIO0 (pin 3, BOOT) and GPIO3 (pin 6) are exposed on castellated pins; GPIO45 and GPIO46 are managed internally.

For more details please read the official documentation of Espressif (ESP32-S3FN8).

3.4 | Pins used

Some GPIOs of the ESP32-S3FN8 are used to handle module features.

- SDA - GPIO8 (RTC, secure element)
- SCL - GPIO9 (RTC, secure element)
- Auto turn off - GPIO14
- Battery level – GPIO7
- Sub-GHz radio (SX1262) SPI bus - GPIO4 (RST), GPIO5 (NSS), GPIO35 (MISO), GPIO36 (MOSI), GPIO45 (SCK), GPIO46 (BUSY), internal only
- Sub-GHz radio DIO1 - GPIO47 (pin 47)

The I²C bus (GPIO8/GPIO9) is shared with the on-board peripherals but remains fully available for user applications; alternatively, a new I²C bus can be created from scratch on any free GPIOs. SDA and SCL include 10 kΩ pull-up resistors to VMCU. Do not drive either line above VMCU or while VMCU is unpowered, unless the external circuit provides suitable isolation against back-powering.

Pins 25 (D-) and 26 (D+) expose the native USB interface of the ESP32-S3 (programming and USB CDC). An external TVS diode on the two USB lines is suggested for ESD protection.

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4 | Electrical characteristics

4.1 | Absolute maximum ratings

Stresses beyond the specified limits may cause permanent damage to the module. These are stress ratings only; functional operation of the module at these or any other conditions beyond the recommended operating conditions is not implied. The maximum permitted voltage at VIN is 5.5 V and the absolute maximum current through PLATCH_DRAIN is 1 A. The application shall operate PLATCH_DRAIN with significant margin below 1 A; this absolute limit is not a guaranteed continuous-current rating. The remaining absolute maximum ratings are under characterization.

4.2 | Recommended operating conditions

To ensure the proper operation of the ELPM-S3LW, the following ranges must be observed.

Symbol	Parameter	Min	Max	Unit
VMCU	Shared 3.3 V rail for ESP32-S3FN8 and ATECC608C; on-board LDO output when supplied from VIN	3.0	3.6	V
I_{VMCU}	Current available to external loads from the VMCU pin	-	235	mA
VIN	Power latch and on-board LDO input	3.0	5.5	V
LDOSUB	LDO2 input	3.0	5.5	V
VSUB	Direct supply rail for the SX1262	1.8	3.7	V
VRTC	Power path for the RTC (RV-3028-C7)	3.0	3.3	V
VIN-LED	Supply input for the addressable RGB LED	3.5	5.5	V

The on-board LDO supplies both the internal ELPM-S3LW circuitry and the external VMCU pin. Operation of the module is guaranteed over the complete 3.0-5.5 V VIN range. When VIN does not provide enough headroom for the LDO, the VMCU rail may fall below its nominal 3.3 V value while the module remains operational. External circuits powered from VMCU must tolerate this reduction.

The 235 mA limit for I_{VMCU} is obtained from the 300 mA LDO rating by reserving 46 mA for the ESP32-S3FN8, up to 14 mA for the ATECC608C and 5 mA of additional margin. This limit assumes the stated 46 mA ESP32-S3FN8 operating profile and sufficient VIN headroom; higher transient consumption, including RF transmit peaks, reduces the current temporarily available to external loads. At low VIN, the external load must be reduced as necessary to keep VMCU within the operating range required by the module and the connected devices. Thermal conditions may require further derating. The LDO dropout is 135 mV typical and 200 mV maximum at 300 mA total rail current; approximately 3.5 V at VIN is therefore required to guarantee a regulated 3.3 V VMCU rail at the maximum total LDO load.

Supplying VRTC from VMCU is the recommended configuration. Although the RV-3028-C7 component supports a wider supply range, the ELPM-S3LW I^2C pull-ups are connected to VMCU and the WAKE2/EVI and RTC_CLK logic levels are referenced to the RTC supply. Therefore, the wider component-only range is not specified as a normal module operating condition. Operation outside the VRTC range shown above requires external level adaptation and system-level verification.

4.3 | Maximum ESD ratings

Module-level ESD immunity is under characterization. No IEC 61000-4-2 system-level rating is claimed in this revision. Most exposed GPIO and control pins connect directly to on-module ICs or logic and do not include dedicated system-level ESD protection.

The SUB_GHz antenna path includes a low-capacitance RF protection device rated at component level for ±14 kV contact discharge and ±18 kV air discharge according to IEC 61000-4-2. These values characterize the protection component only and are not an immunity rating for the complete ELPM-S3LW. External protection must be selected by the integrator according to the accessible interfaces and compliance requirements of the final product.

The VMCU rail also includes an on-module transient-protection device. The protection component is rated for ±12 kV contact discharge and ±15 kV air discharge according to IEC 61000-4-2. These are component-level values and do not constitute an ESD immunity rating for the VMCU rail or for the complete module.

4.4 | Operating temperature range

Parameter	Min	Max	Unit
Operating temperature	-40	+85	°C

4.5 | GPIO DC characteristics

Digital I/O levels of the exposed GPIOs (ESP32-S3FN8 datasheet, VDD = 3.3 V):

Symbol	Parameter	Min	Max	Unit
VIH	High-level input voltage	0.75×VDD	VDD+0.3	V
VIL	Low-level input voltage	-0.3	0.25×VDD	V
VOH	High-level output voltage	0.8×VDD	-	V
VOL	Low-level output voltage	-	0.1×VDD	V

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5 | RF characteristics

The module provides two independent antenna interfaces through U.FL connectors.

Unless otherwise stated, the values in this section are reference values from the ESP32-S3FN8 and SX1262 component datasheets. They describe the capabilities of the integrated radio ICs and are not guaranteed module-level limits. Conducted RF performance of the complete ELPM-S3LW will be added after module characterization.

5.1 | Antenna interfaces

Connector	Radio	Impedance
GHz	WiFi/Bluetooth (ESP32-S3FN8)	50 Ω
SUB_GHz	Sub-GHz radio (SX1262)	50 Ω

5.2 | WiFi and Bluetooth (GHz)

- IEEE 802.11 b/g/n, 2.4 GHz
- Bluetooth 5 (LE), Bluetooth mesh

For component-level RF performance refer to the ESP32-S3 datasheet.

5.3 | Sub-GHz radio (SUB_GHz)

The sub-GHz radio supports LoRa, LoRaWAN and generic sub-GHz protocols. The following are typical component-level values from the Semtech SX1262 datasheet:

Parameter	Condition	Value
Frequency bands	-	862 MHz to 928 MHz
TX output power	configurable	-9 dBm to +22 dBm
LoRa spreading factor	-	SF5 to SF12
LoRa bandwidth	-	7.8 kHz to 500 kHz
LoRa air data rate	-	up to 62.5 kbps
(G)FSK air data rate	-	0.6 kbps to 300 kbps
Sensitivity	LoRa, SF12, BW 10.4 kHz	-148 dBm
Sensitivity	LoRa, SF12, BW 125 kHz	-137 dBm
Sensitivity	LoRa, SF7, BW 125 kHz	-124 dBm
TX current	+22 dBm	118 mA (typ)
RX current	LoRa, BW 125 kHz	4.6 mA (typ)

For detailed component-level RF performance refer to the SX1262 product documentation.

5.4 | Antenna requirements

Both interfaces require 50 Ω antennas connected through the U.FL receptacles. When selecting the antennas, the gain must be chosen so that the radiated power of the final product stays within the regulatory limits of the target region (for example ERP/EIRP limits of the EU 863-870 MHz band and of the 2.4 GHz band).

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6 | Power management

The ELPM-S3LW integrates a smart power unit designed to reduce energy waste from the module and all components powered by it. Deep Stop mode is not intended to replace the deep sleep mode of the ESP32-S3, but is an additional solution that can be tailored during the development of a low-power device.

When the module is supplied through VIN, the on-board LDO generates the shared 3.3 V VMCU rail for the ESP32-S3FN8 and ATECC608C. The regulator is rated for 300 mA total output current and includes current limiting, thermal shutdown and active output discharge. The 300 mA rating includes the on-module VMCU loads and must not be interpreted as fully available external current.

The module remains operational throughout the specified 3.0-5.5 V VIN range. Near the lower end of this range, VMCU may be below its nominal 3.3 V value because of the LDO dropout. External loads supplied from VMCU must accept the resulting rail voltage and must be derated when necessary.

For local VMCU decoupling, 10 μF and 1 μF capacitors in parallel are recommended close to the module pin. A local bulk capacitor at VIN is also recommended when the supply connection is long or the source has appreciable impedance. Final mandatory capacitance requirements are subject to module-level validation.

6.1 | Supply configurations

The power pins support the following supply configurations. MCU-domain and radio-domain configurations may be combined where the stated voltage and logic-level requirements are satisfied.

Configuration	Connections	Pins left floating
VIN power latch, MCU only	Apply 3.0-5.5 V to VIN; VMCU is an output	Do not drive VMCU; leave LDOSUB and VSUB floating
VIN power latch, switched radio	Apply 3.0-5.5 V to VIN; connect PLATCH_DRAIN to LDOSUB	Do not drive VMCU; leave VSUB floating
VIN power latch, always-on radio	Apply 3.0-5.5 V to VIN; supply LDOSUB independently from the battery/source	Do not drive VMCU; leave VSUB floating
Direct MCU supply	Apply regulated 3.3 V to VMCU	Leave VIN floating
Direct regulated radio supply	Short LDOSUB and VSUB together and apply 3.0-3.7 V; supply VMCU separately or from the same compatible source	Leave VIN floating when VMCU is supplied directly

VRTC, VIN-LED, LDOSUB and VSUB are dedicated supply inputs and shall not be used as power outputs for external circuitry. A dedicated input may be left unconnected when the corresponding on-module function is not required: leave VRTC unpowered to disable the RTC domain, VIN-LED unpowered to disable the RGB LED, and both LDOSUB and VSUB unpowered to disable the Sub-GHz radio. VRTC may instead remain supplied while the main MCU domain is off, and VIN-LED may be switched according to the required RGB LED behaviour and standby-current target. Neither VRTC nor VIN-LED changes the required VIN/VMCU or LDOSUB/VSUB connections shown above.

The configurations are detailed below:

- **Power-latch mode:** apply the supply to VIN. The on-board LDO then generates VMCU for the ESP32-S3FN8 and ATECC608C, and VMCU may also supply external loads within the current limit specified in Section 4. Do not drive VMCU from an external source in this configuration.

- **Direct MCU supply:** apply a regulated 3.3 V supply to VMCU and leave VIN floating. This bypasses the power-latch path and directly supplies the ESP32-S3FN8 and ATECC608C rail.
- **RTC wake source:** keep VRTC supplied while the main power latch is off. A programmed RTC timer/alarm or an external event on WAKE2/EVI can then assert the RTC interrupt connected to the power-latch wake path. The module has no internal RTC backup battery, so removing VRTC stops timekeeping and loses the stored date and time.
- **Sub-GHz radio through its on-board LDO:** apply the radio supply to LDOSUB and leave VSUB floating. LDOSUB may be connected directly to the battery when the radio must remain powered, or to PLATCH_DRAIN when the radio must be powered only while the power latch is active. PLATCH_DRAIN has a 1 A absolute maximum path current, but external loads shall be designed to remain significantly below this value.
- **Direct regulated Sub-GHz supply:** short LDOSUB and VSUB together and connect them to the same external regulated source. VMCU may be supplied by a separate source, or it may be connected to the same regulated source when that source remains within the operating ranges of all connected rails and has sufficient current capability. The SX1262 supply range is 1.8 V to 3.7 V, but the effective source range must also satisfy the LDOSUB input limits and SPI logic-level requirements. The maximum RF output power depends on the SX1262 supply voltage. When separate supplies are used, the SPI logic levels between the ESP32-S3FN8 and SX1262 must remain valid in every operating and power-transition state.

PLATCH_DRAIN is an unregulated switched copy of VIN. When the power latch is active, its voltage is nominally equal to VIN apart from the small voltage drop of the internal path; it must not be treated as a precision regulated supply. The internal switching implementation is not part of the module interface specification.

When the power latch is off, PLATCH_DRAIN is high-impedance and is not actively discharged. Its decay time therefore depends on the connected load and external capacitance. Applications requiring a defined or rapid discharge shall provide a suitable external discharge path.

6.2 | Power consumption

Unless otherwise stated, measured values in this section were obtained from engineering samples at 3.3 V and room temperature. Typical values characterize the tested samples and are not production-tested limits.

Work mode	Description	Temp	Vin	Reference value	Unit
Deep Stop (RTC disabled)	MASTER, GATE or WAKE input triggering the power latch. RTC not powered.	+20°C to +30°C	3.3V	1--30	nA
Deep Stop with RTC	RTC powered. Multiple interrupt sources.	+20°C to +30°C	3.3V	45--100	nA
Deep sleep	Default deep sleep mode of the ESP32-S3.	+20°C to +30°C	3.3V	6--10	µA
Active	MCU running at 240 MHz, radios idle (measured).	+20°C to +30°C	3.3V	46	mA
Sub-GHz TX[a]	SX1262 transmitting @ +22 dBm.	+25°C	3.3V	118	mA
Sub-GHz RX[a]	SX1262 receiving (LoRa, BW 125 kHz).	+25°C	3.3V	4.6	mA

[a] Radio contribution only (SX1262 datasheet values): add the MCU current of the active work mode. For the WiFi and Bluetooth LE consumption refer to the ESP32-S3 datasheet.

6.3 | Auto turn off (power latch control)

Only when the system is supplied from VIN through the power latch, firmware controls the shutdown via the AUTO TURN OFF signal (GPIO14). In this supply mode, configuring GPIO14 as an output and driving it high must be one of the first firmware operations after the MCU starts, before peripheral initialization or other potentially time-consuming tasks. The signal must remain high for the entire powered phase; driving it low requests shutdown through the power latch. If AUTO TURN OFF is not asserted early enough, the power latch may remove the supply before startup completes. While AUTO TURN OFF is held high, it forces the power latch to remain on and subsequent events on MASTER, WAKE or GATE are ignored. These inputs become effective again after the controlled shutdown has released the latch.

When the module is supplied directly through VMCU, the power-latch path is bypassed and the state of AUTO TURN OFF does not control the module supply. GPIO14 does not need to be asserted to keep the system powered, and driving it low does not turn off the external VMCU source.

6.4 | Sub-GHz packet wake-up

The exposed LORA_DIO1 pin may be connected externally to PLATCH_MASTER to turn on the power latch when the SX1262 asserts DIO1, for example after a valid packet reception. This configuration has been functionally verified on engineering hardware. The radio must be configured before shutdown so that the required IRQ is routed to DIO1, and the SX1262 supply, including its VBAT_IO domain, must remain active while waiting for the event. After startup, AUTO TURN OFF is held high and forces the latch on; consequently, the opposite MASTER edge produced when firmware clears the radio IRQ and DIO1 returns inactive is ignored and does not disturb the powered state.

Before turning the ESP32-S3FN8 off, firmware should configure the connected SPI and control GPIOs as inputs with internal pulls disabled whenever permitted by the radio state. This reduces actively driven paths during shutdown but does not provide galvanic isolation: after VMCU is removed, the ESP32-S3FN8 no longer retains the software GPIO configuration and an active SX1262 output may inject current through an unpowered ESP32-S3FN8 pad. Consequently, this packet-wake configuration does not carry the nanoampere Deep Stop current specification; its total off-state current includes the selected SX1262 receive mode and any residual interface current. Hardware isolation is required when guaranteed elimination of interface back-powering is needed.

6.5 | Startup time

The power latch is capable of booting the whole system in a few milliseconds, ensuring high reactivity. It is possible to reduce the startup time of the ESP32-S3 by tuning the boot options.

Interrupt mode	Description	Typ	Unit
MASTER P.Latch	Change of input status.	30	ms
RTC WAKE	Scheduled wake-up.	80	ms
GATE	GATE input to GND.	20	ms
WAKE	WAKE input to GND.	500	ms

ESP32-S3FN8	Typ	Unit
Default startup time	105	ms

6.6 | Deep Stop performance

The following charts were measured with a Qoitech Otii Arc power analyzer at 4000 samples/s. They show the wake-up times from Deep Stop and the consumption of the module when used in combination with the integrated RTC, with scheduled wake-up intervals that can be reconfigured via software, even at every power-on.

6.6.1 | MASTER input cycle

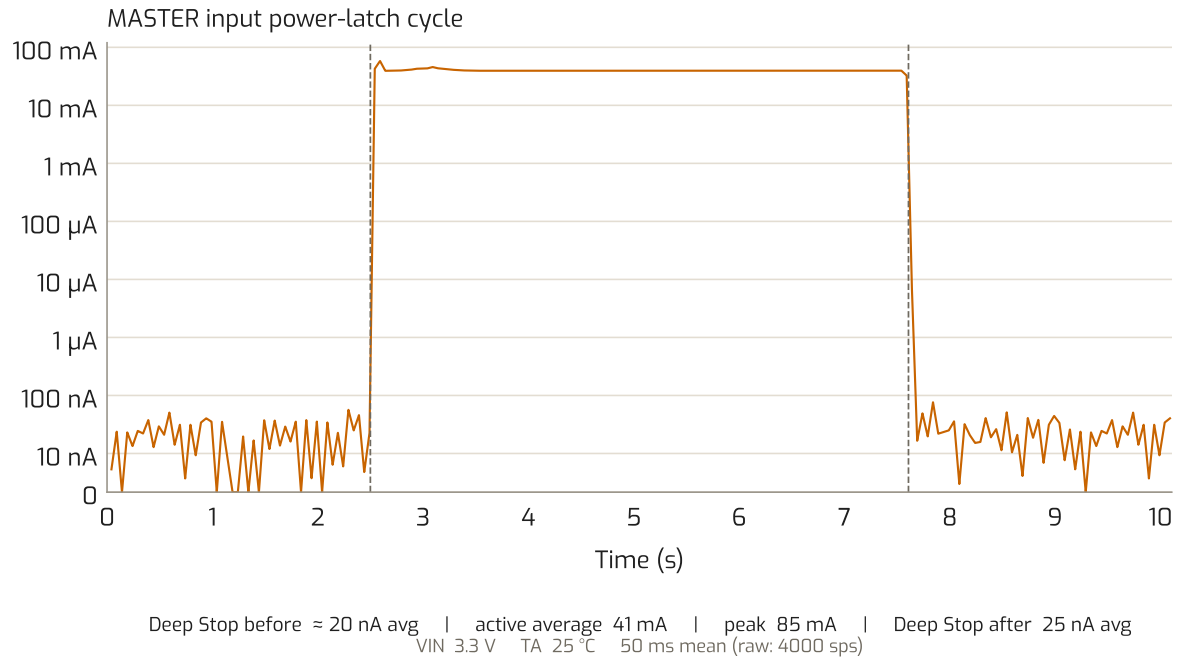

Figure 6.1: Startup from a MASTER input transition, active phase, controlled shutdown and measured decay toward Deep Stop (logarithmic current axis).

6.6.2 | WAKE input cycle

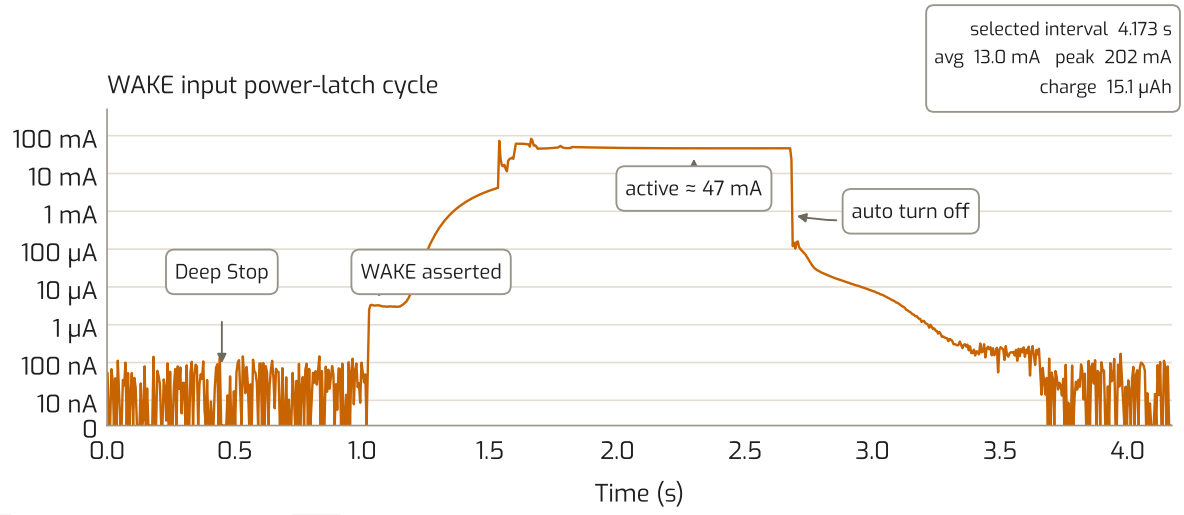

Figure 6.2: Deep Stop with the RTC disabled and wake-up from the WAKE input (logarithmic current axis).

6.6.3 | RTC mode

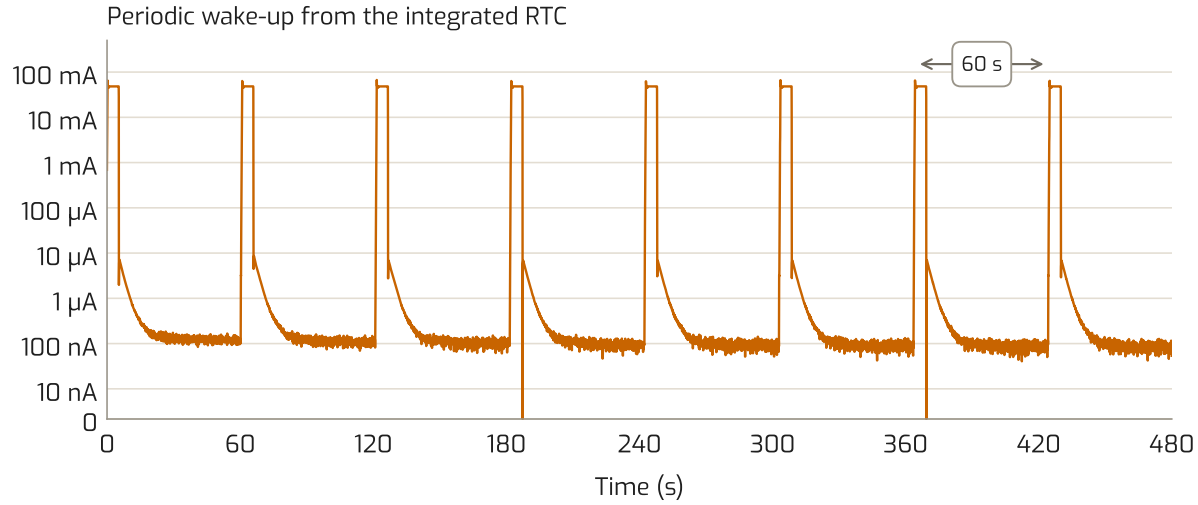

Figure 6.3: Wake-up every minute from the integrated RTC, nine consecutive cycles (logarithmic current axis).

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7 | On-board peripherals

The module integrates the following peripherals: the RTC and the secure element, sharing the same I²C bus (SDA: GPIO8, SCL: GPIO9) with integrated 10 kΩ pull-up resistors to VMCU, the RGB status LED (WS2812B) and the battery level circuit.

7.1 | I²C address map

Device	Function	I²C address
RV-3028-C7	Real time clock	0x52
ATECC608C	Secure element	0x60

The on-board pull-up resistors are referenced to VMCU. External devices on this bus must not drive SDA or SCL above VMCU or while VMCU is unpowered, unless suitable isolation is provided to prevent back-powering.

7.2 | RTC (RV-3028-C7)

Extreme low power external real time clock (45 nA to 100 nA), used by the Deep Stop mode for scheduled or event-driven wake-up. It features a dedicated power supply pad (VRTC), a clock output (RTC_CLK pin) and an external event input (WAKE2, connected to the RV-3028-C7 EVI pin).

When VRTC is supplied, the RTC can assert its interrupt output either from an internally programmed timer/alarm or from an event detected on WAKE2/EVI. The RTC interrupt is connected internally to the wake path of the power latch. For example, a one-minute periodic timer produces one interrupt and one system startup every minute. Alternatively, WAKE2 allows an external signal to use the same RTC interrupt path and may also use the RTC event-detection and time-stamp functions. WAKE2 includes an on-module 10 kΩ pull-down resistor and does not require an external resistor to define its inactive state. Configure the RTC event input for an active-high level or rising-edge event; active-low operation is not supported as a module configuration because the pull-down defines low as the normal inactive state. Do not drive WAKE2 above VRTC or while VRTC is unpowered. WAKE2-based wake-up is unavailable when VRTC is not powered. Event filtering, interrupt routing and flag clearing must be configured through the RTC registers as described in the RV-3028-C7 application manual.

The ELPM-S3LW does not include an internal backup battery for the RTC. VRTC must remain externally supplied to preserve timekeeping while the main system is off; removing VRTC stops the RTC and the stored date and time are lost.

Connecting VRTC to VMCU is recommended. The on-board I²C pull-ups are tied to VMCU, while the RTC input thresholds depend on VRTC; consequently, supplying the RTC above the specified module VRTC range requires suitable level adaptation for I²C and the other RTC-domain signals.

7.3 | Secure element (ATECC608C)

The ATECC608C is a secure element providing hardware-based secure key storage and cryptographic acceleration: ECDSA sign/verify and ECDH key agreement on the ECC P-256 curve, SHA-256, AES-128 and monotonic counters. The module mounts the standard I²C version of the device, shipped unprovisioned: key slots and configuration are fully available and their use is entirely at the discretion of the end user. When the secure element is correctly configured and locked, private keys generated in non-readable slots remain inside the device and cryptographic operations involving them are executed in hardware. Provisioning, access policies and configuration locking are the responsibility of the end user.

7.3.1 | Module authenticity

During provisioning the end user can give each module a unique cryptographic identity: a device certificate whose private key is generated and locked inside the secure element. The infrastructure can then verify possession of that identity through a challenge-response mechanism: the module

signs a random challenge with its private key and the verifier checks the signature against the device certificate chain. This authenticates the provisioned device identity; system-level tamper resistance depends on the complete product design and provisioning process.

7.3.2 | Example: MQTT with mutual TLS

An MQTT broker can be configured to require mutual TLS (mTLS): the module authenticates itself during the TLS handshake by signing with the private key stored in the ATECC608C, and access to specific topics can be restricted to authenticated clients only. Since the private key cannot be extracted or duplicated, the client identity cannot be forged.

7.3.3 | Sub-GHz security layer

The secure element also benefits the sub-GHz radio. For LoRaWAN the user can store the root keys in the device and use it to compute the AES-CMAC message integrity code. For proprietary sub-GHz protocols, transmitted messages can be signed (ECDSA) or authenticated (AES-CMAC), guaranteeing the authenticity and integrity of every frame and protecting the network from spoofing and tampering; monotonic counters can be used to prevent replay attacks.

7.3.4 | Regulatory context

The hardware root of trust provided by the secure element (unique device identity, protected key storage, verification of update authenticity) gives the final product a solid hardware foundation to meet the essential cybersecurity requirements of the EU Cyber Resilience Act (Regulation (EU) 2024/2847).

7.4 | RGB status LED (WS2812B-1010)

The addressable RGB LED is connected to GPIO48, located under the X of the logo and powered independently through the VIN-LED input. VIN-LED accepts 3.5-5.5 V. The LED specifies a 2.8 V minimum DIN high threshold at VIN-LED = 5.0 V, allowing direct control from the 3.3 V GPIO48 at this supply voltage. Operation at VIN-LED = 5.5 V with direct 3.3 V control is not characterized by the LED manufacturer and shall be verified in the final application or implemented with level translation. Full white draws approximately 15 mA from VIN-LED, in addition to the control-circuit current.

The DOUT pin of the on-module LED is not connected or exposed. When GPIO48 is also used to drive external addressable LEDs, the DIN inputs of the on-module LED and the first external LED are driven in parallel. This is a supported configuration and does not create a data conflict: both LEDs decode the same first pixel and therefore display the same colour. Further external LEDs may be cascaded from the DOUT pin of the first external LED in the usual manner.

VIN-LED may remain supplied while VMCU is off, but the LED then remains powered and draws approximately 0.35 mA typical with all colour channels off. For minimum-power operation, switch VIN-LED off together with the module. Before removing VIN-LED while VMCU remains supplied, configure GPIO48 low or as a high-impedance input: DIN must not be driven above VIN-LED by more than 0.4 V. The same low or high-impedance state is recommended before a power-latch shutdown to avoid power-sequencing transients.

7.5 | Battery level

The battery-level input is connected to GPIO7 through a resistive divider made of two 100 kΩ resistors. The divider ratio is 1:2, therefore the nominal voltage at GPIO7 is half the battery voltage:

$$V_{\text{GPIO7}} = \frac{V_{\text{BAT}}}{2}.$$

The divider presents a nominal 50 kΩ Thevenin source resistance to the ADC and draws $V_{\text{BAT}}/200\,\text{k}\Omega$ from the monitored supply. ADC acquisition time, attenuation and calibration shall be selected accordingly.

8 | Software support

The module is based on the ESP32-S3 and is fully compatible with its standard development ecosystem: Arduino IDE, PlatformIO and ESP-IDF.

Engineering samples are shipped with a basic RGB status LED rainbow firmware for functional indication. This test firmware is not locked, may be completely replaced by the user and will be published through the official repository. Firmware development remains ongoing; this statement does not claim that every module feature or power-latch workflow is already implemented by the factory test firmware.

Ready-to-use firmware examples are available and maintained in the official OBJEX Labs GitHub repository:

github.com/OBJEX-Labs/OBJEX_ELPMs

Available examples:

- RGB status LED
- Power latch: MASTER/WAKE inputs and auto turn off
- Power latch: RTC scheduled wake-up
- LoRaWAN node (RadioLib)
- LoRa point-to-point (ping-pong)

OBJEX also provides a dedicated support library that manages the on-board peripherals (RTC, RGB status LED, secure element, power latch) and other module features, and includes drivers for sensors commonly used with the module. The library does not constrain the development environment chosen by the user: it is a convenience layer to control the module in the most efficient way, and can be used alongside any of the supported ecosystems.

The GPIOs reserved for the module features are listed in Section 3.4.

8.1 | Power-latch startup requirement

When the module is supplied from VIN and starts through the power latch, firmware must configure GPIO14 (AUTO TURN OFF) as an output and drive it high as one of its first operations. This must occur before peripheral initialization, network startup or other potentially time-consuming tasks. Keep GPIO14 high for as long as the system must remain powered and drive it low only to request the controlled shutdown described in Section 6.3. This requirement does not apply when the module is supplied directly through VMCU: in direct-supply mode, AUTO TURN OFF does not control the external VMCU source.

8.2 | Programming interfaces

The module includes an on-board pull-up on RESET, so the ESP32-S3 starts normally when power is applied without requiring an external reset pull-up or reset controller. RESET remains available on pin 2 for manual reset and programming control.

The module can be programmed through two interfaces:

- **UART0**: TXD (pin 56) and RXD (pin 55). To enter the serial download mode, hold BOOT (pin 3) low while releasing RESET (pin 2).
- **Native USB**: D- (pin 25) and D+ (pin 26), exposing the built-in USB Serial/JTAG controller of the ESP32-S3 (programming, USB CDC console and JTAG debug). An external TVS diode on the two USB lines is suggested.

Both interfaces are supported by the standard Espressif flashing tools (esptool, Arduino IDE, PlatformIO, ESP-IDF).

9 | Typical applications

The following reference schematics show typical supply configurations of the ELPM-S3LW.

9.1 | Direct constant supply

Apply a regulated 3.3 V supply to VMCU and leave VIN floating. This directly supplies the ESP32-S3FN8 and ATECC608C and bypasses the power-latch path.

To power the Sub-GHz radio from the same regulated 3.3 V source, connect VMCU, LDOSUB and VSUB together and connect the common node to the source. LDOSUB and VSUB must both be connected in this direct-supply configuration. If the Sub-GHz radio is not required, leave both LDOSUB and VSUB unconnected.

VRTC may also be connected to the same 3.3 V source when RTC operation is required. VIN-LED requires 3.5-5.5 V and shall therefore remain unconnected or use a separate compatible source in this 3.3 V configuration.

Schematic: TBD.

9.2 | Battery supply with power latch and external wake source

Battery powered through the power latch: an external source triggers a power-latch input and turns the system on only when an event occurs. The source may be a sensor, a switch, a logic output or any other circuit that produces the required voltage transition. MASTER reacts to either change of input state, while WAKE and GATE shall be driven according to their specified active levels.

If the Sub-GHz radio must follow the same switched power state, connect PLATCH_DRAIN to LDOSUB and leave VSUB floating. To keep the radio powered independently, connect the battery supply to LDOSUB instead.

Schematic: TBD.

9.3 | Battery supply with power latch and periodic RTC wake-up

Battery powered through the power latch: a sensor (for example a temperature sensor) is switched off together with the system and read at each periodic wake-up scheduled by the RTC. VRTC must remain supplied while the main system is off. The same wake path may instead be activated by an external event connected to WAKE2/EVI, after enabling and configuring the RTC event interrupt.

Schematic: TBD.

9.4 | Sub-GHz packet wake-up

Keep the SX1262 supply active and connect the exposed LORA_DIO1 pin to PLATCH_MASTER. When the radio is configured to route a packet-reception IRQ to DIO1, the DIO1 transition activates the power latch and starts the ESP32-S3FN8. This mode keeps the radio and its I/O supply active and therefore has a higher off-state current than Deep Stop with the radio disabled; see Section 6.4.

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10 | Design guidelines

10.1 | Module placement and layout

- Follow the recommended PCB footprint (Section 11.4).
- Do not route signal traces or place vias on the top layer of the host board under the module body: keep the area limited to the footprint pads and to a solid ground pour.
- Connect the castellated GND pins to a solid ground plane. The auxiliary bottom VIN and GND contacts are optional and are primarily intended for point-to-point or minimal-carrier assemblies.
- Leave enough clearance around the castellated edges for soldering inspection and rework.
- Keep the area around the two U.FL receptacles clear, so that the coaxial plugs can be mated and the cables routed without stress.

The RF shield can is electrically connected to module GND. Do not use the shield can as a power or signal connection, and prevent conductive mechanical parts from applying unintended current through it.

10.2 | Antenna connections

Both RF interfaces use the same standard U.FL coaxial receptacle (50 Ω) soldered on the module. To connect the antennas, use 50 Ω cable assemblies terminated with a standard U.FL mating plug (Hirose U.FL-LP series or compatible). Note that this connector family is rated for a limited number of mating cycles (typically 30): use the dedicated extraction tool and avoid unnecessary connect/disconnect cycles.

10.3 | External circuitry

- USB: an external TVS diode on the D+/D- lines (pins 25/26) is suggested for ESD protection.
- Exposed signals: add application-appropriate ESD protection to GPIOs, control inputs and other interfaces that are accessible in the final product.
- WAKE/MASTER inputs: maximum 3.3 V, driven through a high value resistance to GND (never floating); keep the traces short to avoid spurious wake-up events.
- WAKE2/EVI: an on-module 10 kΩ pull-down defines the inactive state. Configure the RTC for an active-high level or rising-edge event. Keep the applied level within the VRTC domain and do not drive the pin while VRTC is unpowered.
- Power input: place a local bulk capacitor close to the VIN pin when the supply cable is long or the battery has a high internal resistance.
- PLATCH_DRAIN loads: the 1 A value is an absolute maximum for the switched path, not a recommended continuous operating current. Design external loads with significant current and thermal margin.
- VMCU decoupling: place 10 μF and 1 μF capacitors in parallel close to the VMCU pin, using short connections to the ground plane.
- Separate VMCU and Sub-GHz supplies: ensure that the SPI input levels remain valid for both devices during normal operation, startup and shutdown. Prevent an active SPI signal from unintentionally powering an unpowered rail through an I/O pin.
- Optional supply domains: VIN-LED, VRTC, LDOSUB and VSUB are inputs only and shall not supply external loads. Leave the corresponding input unconnected when the RGB LED, RTC or Sub-GHz radio is not required.

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10.4 | Configurable host-board power routing

For host boards intended to support multiple product configurations, use individually populated 0 Ω links to select the source of VRTC, VIN-LED and the Sub-GHz supply path. This allows one PCB layout to support, for example, an always-on or switched RTC, an optional RGB LED supply, and an always-on, power-latch-controlled or externally regulated Sub-GHz radio.

Place the links so that each supply path can be inspected and reconfigured independently. Mutually incompatible links shall not be populated at the same time: in particular, do not connect an external source to VMCU while VIN is supplying the on-board LDO, and do not connect independent sources to LDOSUB and VSUB when those two pins are linked for direct radio supply. The voltage range and power-sequencing requirements of every selected configuration remain applicable.

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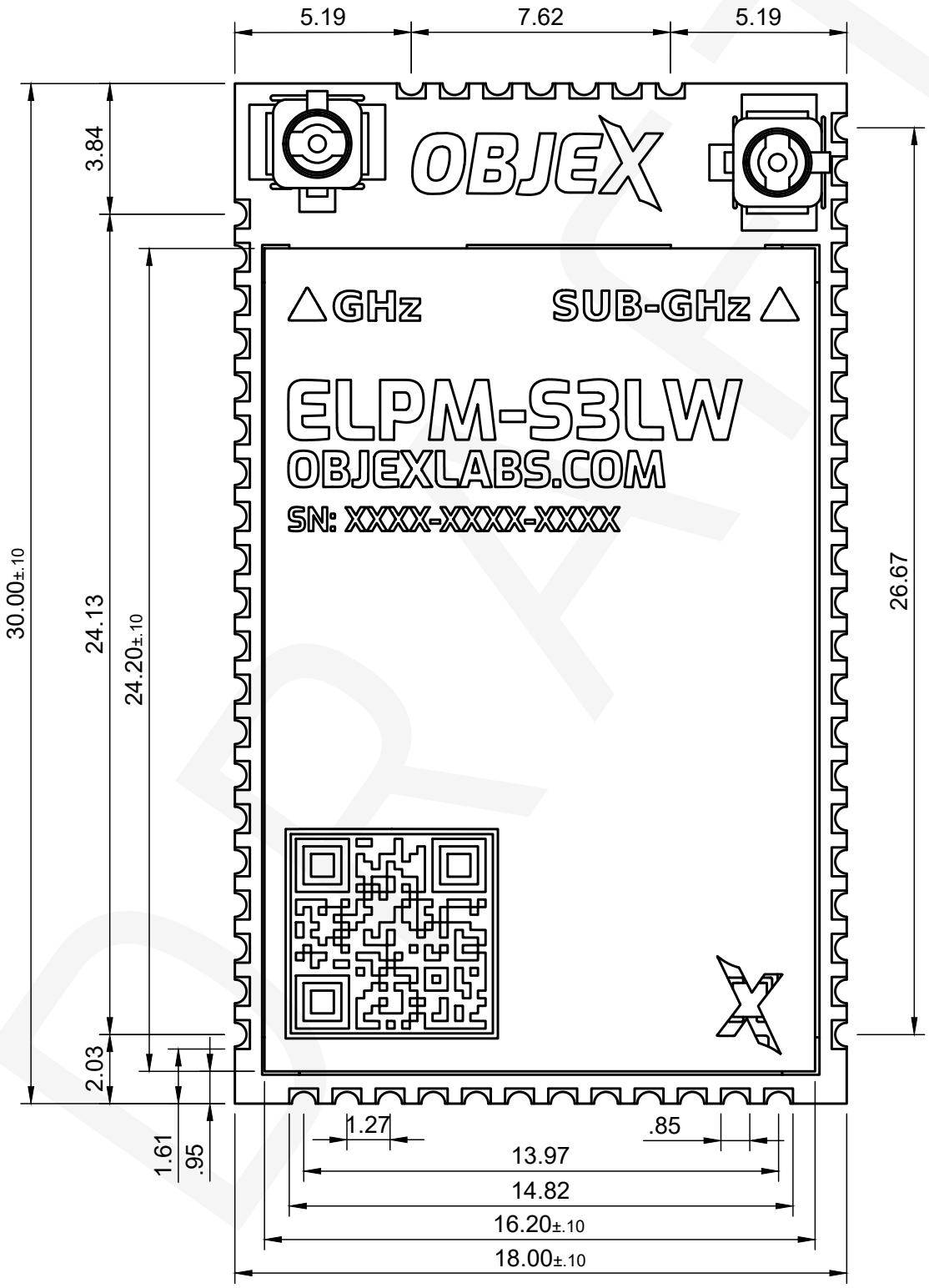
11 | Physical Dimensions

Dimensions in millimeters.

11.1 | Top view



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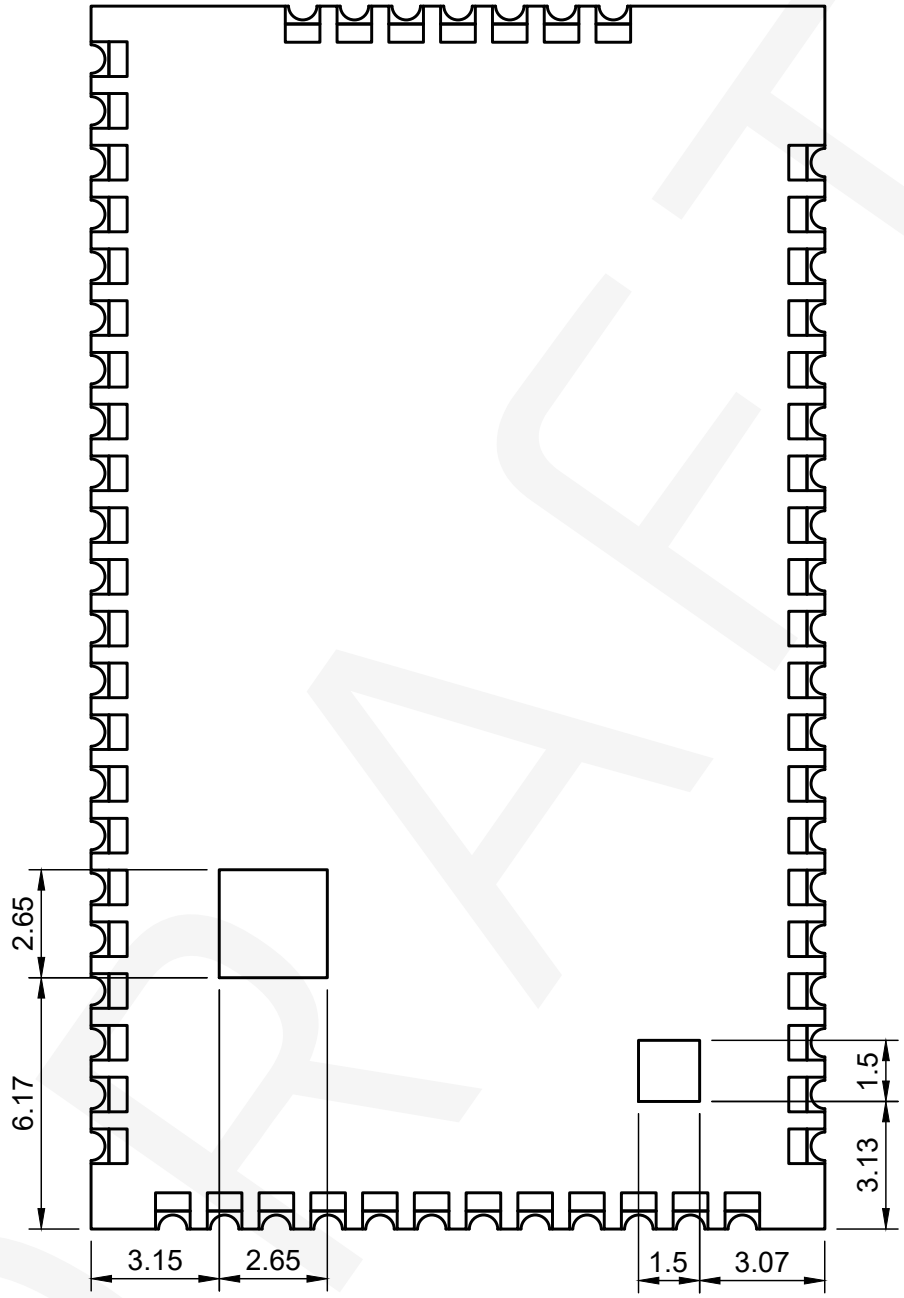
11.2 | Bottom view



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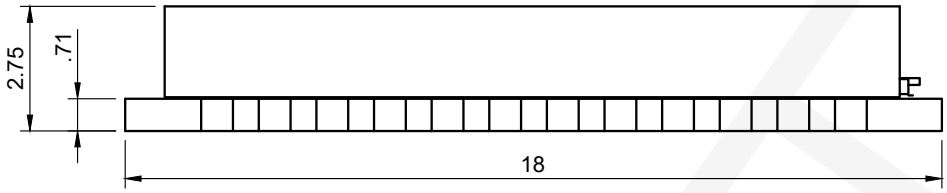
11.3 | Side view



11.4 | Recommended PCB footprint

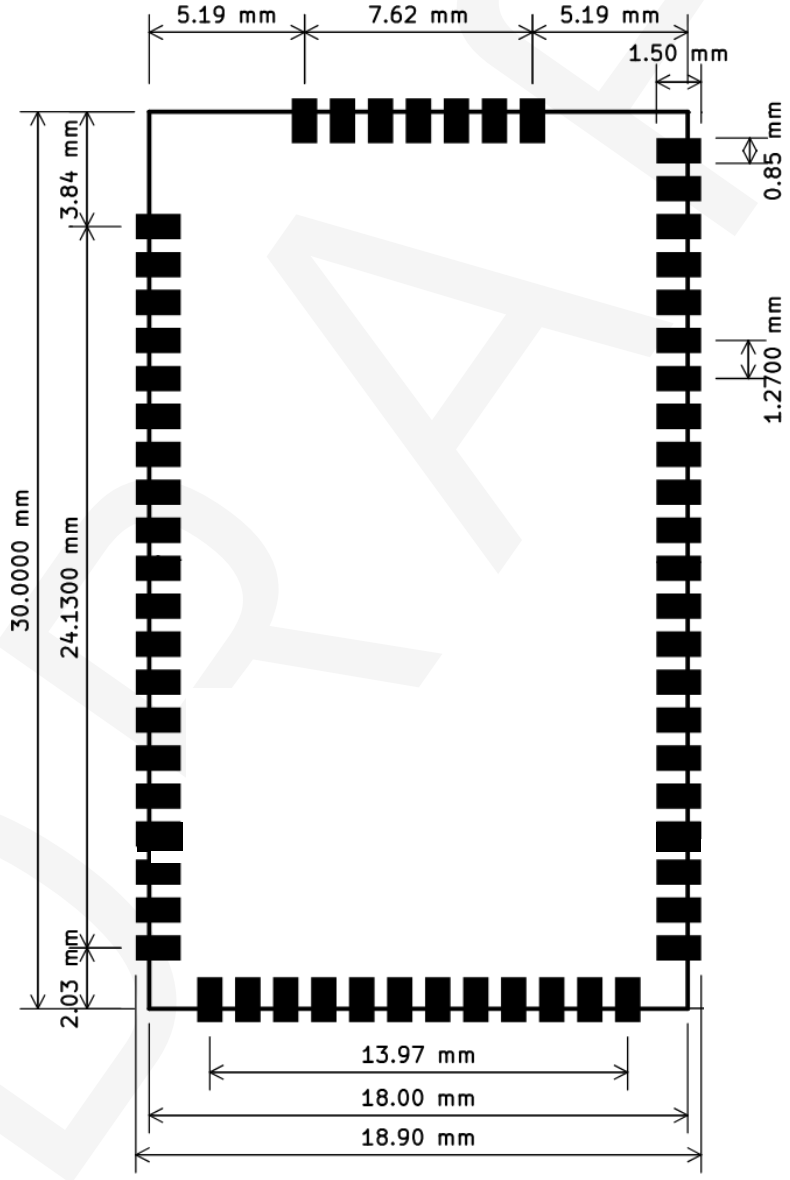


Figure 11.1: Recommended host-PCB footprint. Auxiliary underside VIN and GND contacts are intentionally omitted.

12 | Soldering and handling

12.1 | Reflow soldering

The module contains lead-free SAC-type internal solder joints with a liquidus temperature of approximately 217 °C. These joints shall not be allowed to reflow during host-board assembly. Use a low-temperature lead-free solder paste suitable for the host PCB and keep the temperature measured on the module below 217 °C throughout the complete process. A SnBi- or SnBiAg-based process is recommended.

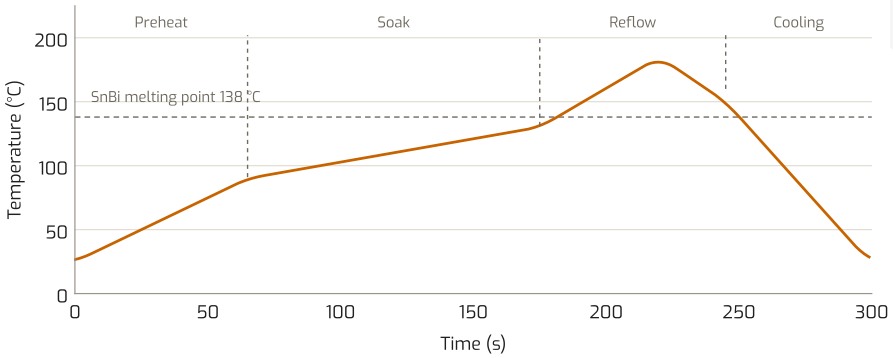


Figure 12.1: Recommended low-temperature reflow profile.

Profile parameter	Recommended value
Ramp-up rate	≤ 2 °C/s
Preheat/soak	60 s to 120 s, 90 °C to 130 °C
Peak temperature	170 °C to 190 °C
Time above paste liquidus	45 s to 90 s
Ramp-down rate	≤ 3 °C/s
Maximum reflow cycles	2

The values above are starting limits for process development, not a substitute for the selected solder-paste specification. Validate the profile on the actual host assembly using a thermocouple attached to the module, accounting for PCB size, copper distribution, component loading and oven characteristics. A conventional high-temperature SAC reflow profile is not supported for host-board assembly because it can reflow the module's internal joints. If the required joint quality cannot be achieved while respecting these limits, use a selective or hand-soldering process instead.

12.2 | Moisture sensitivity

Engineering samples have not been assigned a moisture sensitivity level. They are supplied in sealed ESD-protective bags; this packaging shall not be interpreted as qualified moisture-barrier packaging. Floor-life and baking conditions are not specified in this revision and will be defined only after module-level qualification according to J-STD-020 and handling-process validation according to J-STD-033.

12.3 | Storage conditions

Keep engineering samples in their sealed ESD-protective bags and store them in a dry, non-condensing environment, protected from corrosive atmospheres, direct sunlight and rapid temperature changes. No qualified temperature, humidity or shelf-life limit is assigned in this revision.

12.4 | ESD handling precautions

The module is an electrostatic discharge sensitive device. Handle it only at ESD-protected workstations (grounded wrist strap, dissipative surfaces) in accordance with IEC 61340-5-1 or ANSI/ESD S20.20, and keep it in its original protective packaging until assembly.

13 | Ordering information

Preliminary: order codes and packaging details will be finalized before mass production.

Order code	Description	Packaging
ELPM-S3LW-R16B	Revision 1.6, 868-925 MHz Sub-GHz band variant	Engineering samples: sealed ESD bag

13.1 | Product marking

Each engineering sample is marked on the top overlay with the product name, the manufacturer website and a unique serial number. The serial-number format is illustrated by EGSE-SL26-B475: EGSE identifies an engineering sample, SL identifies the S3LW module, 26 is the production year, B identifies the 868-925 MHz Sub-GHz band variant and 475 is an incremental unit number. The QR code encodes exactly the same serial-number string, allowing fast identification and unit-level traceability.

14 | Certifications

Certification activities are in progress: internal verification is being completed before laboratory testing. The table below will be updated as the activities progress.

Certification	Region	Status
CE (RED)	Europe	In progress

14.1 | Material compliance (RoHS, REACH)

The module is designed and manufactured to comply with Directive 2011/65/EU (RoHS 2) as amended by Directive (EU) 2015/863, and with Regulation (EC) 1907/2006 (REACH). Compliance declarations will be made available together with the product certifications.

14.2 | WEEE (RAEE)

In accordance with Directive 2012/19/EU on waste electrical and electronic equipment (WEEE, implemented in Italy as RAEE), this product must not be disposed of with unsorted municipal waste at the end of its life. The crossed-out wheeled bin symbol indicates that the product is subject to separate collection: return it to an authorized collection point or to the distributor for proper treatment, recovery and recycling.

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15 | Related documentation

- ESP32-S3 Series - Microcontroller
- ESP32-S3 Hardware Design Guidelines - Hardware integration
- ESP32-S3 Series SoC Errata - Known issues and revisions
- SX1262 - Sub-GHz radio IC
- RV-3028-C7 - Extreme low power ext. RTC
- ATECC608C - Secure element
- WS2812B-1010 - RGB status LED

16 | Acronyms

- **ADC** - Analog to Digital Converter
- **BLE** - Bluetooth Low Energy
- **CDC** - Communications Device Class (USB)
- **EIRP** - Effective Isotropic Radiated Power
- **ERP** - Effective Radiated Power
- **ESD** - Electrostatic Discharge
- **(G)FSK** - (Gaussian) Frequency Shift Keying
- **GPIO** - General Purpose Input/Output
- **LDO** - Low Dropout regulator
- **MSL** - Moisture Sensitivity Level
- **mTLS** - mutual Transport Layer Security
- **NC** - Not Connected
- **RTC** - Real Time Clock
- **SF** - Spreading Factor (LoRa)
- **TVS** - Transient Voltage Suppressor
- **WEEE** - Waste Electrical and Electronic Equipment

17 | Revision history

Revision	Date *(ISO 8601)*	Description
v1.6	2026-08-12	Hardware revision: ATECC608C secure element added, U.FL nomenclature updated (GHz, SUB_GHz), pin naming and placement updates. Document restructured and fully revised
v1.1	2024-07-06	Added example firmware section
v1.1	2024-04-18	Added power consumption graphs and general corrections (draft)
v1.0	2024-03-05	Updated frequency band to 862 MHz to 928 MHz
v1.0	2024-02-26	Preliminary version for partners

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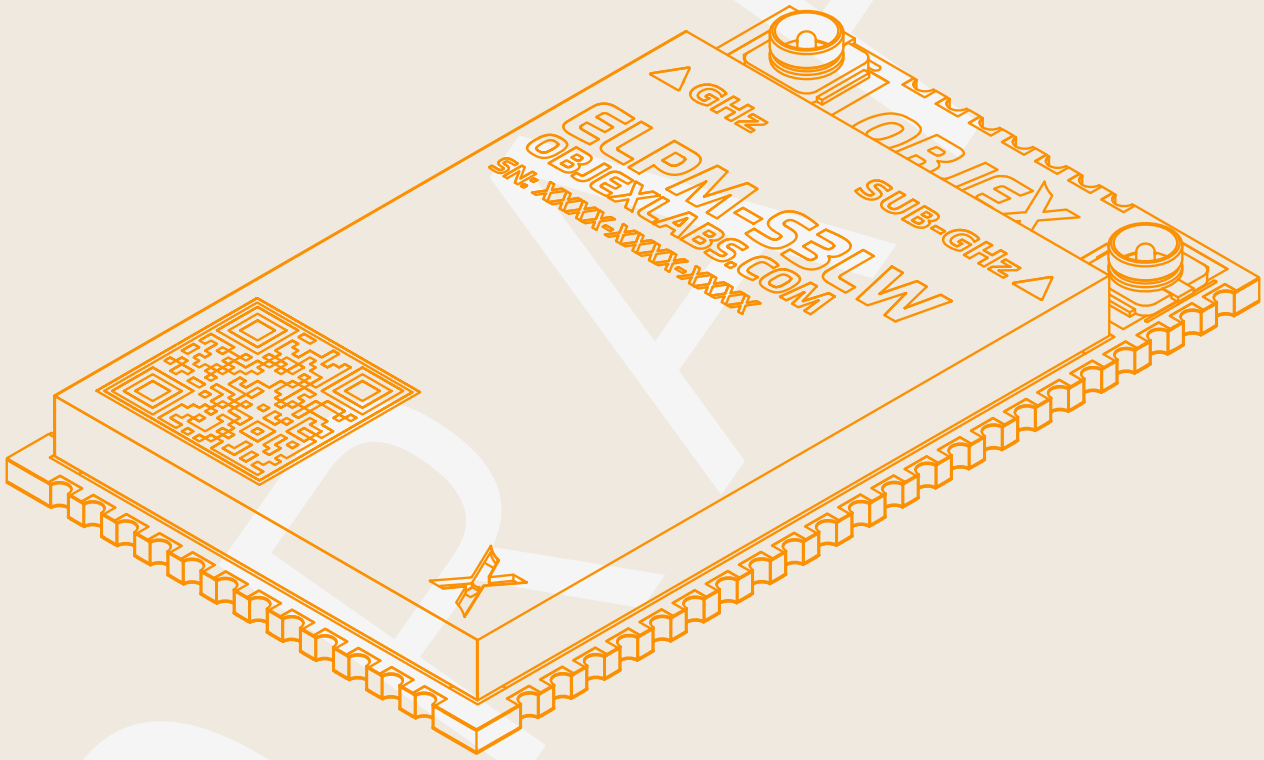

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